

Modeling & Simulation for Signal Integrity & EMI

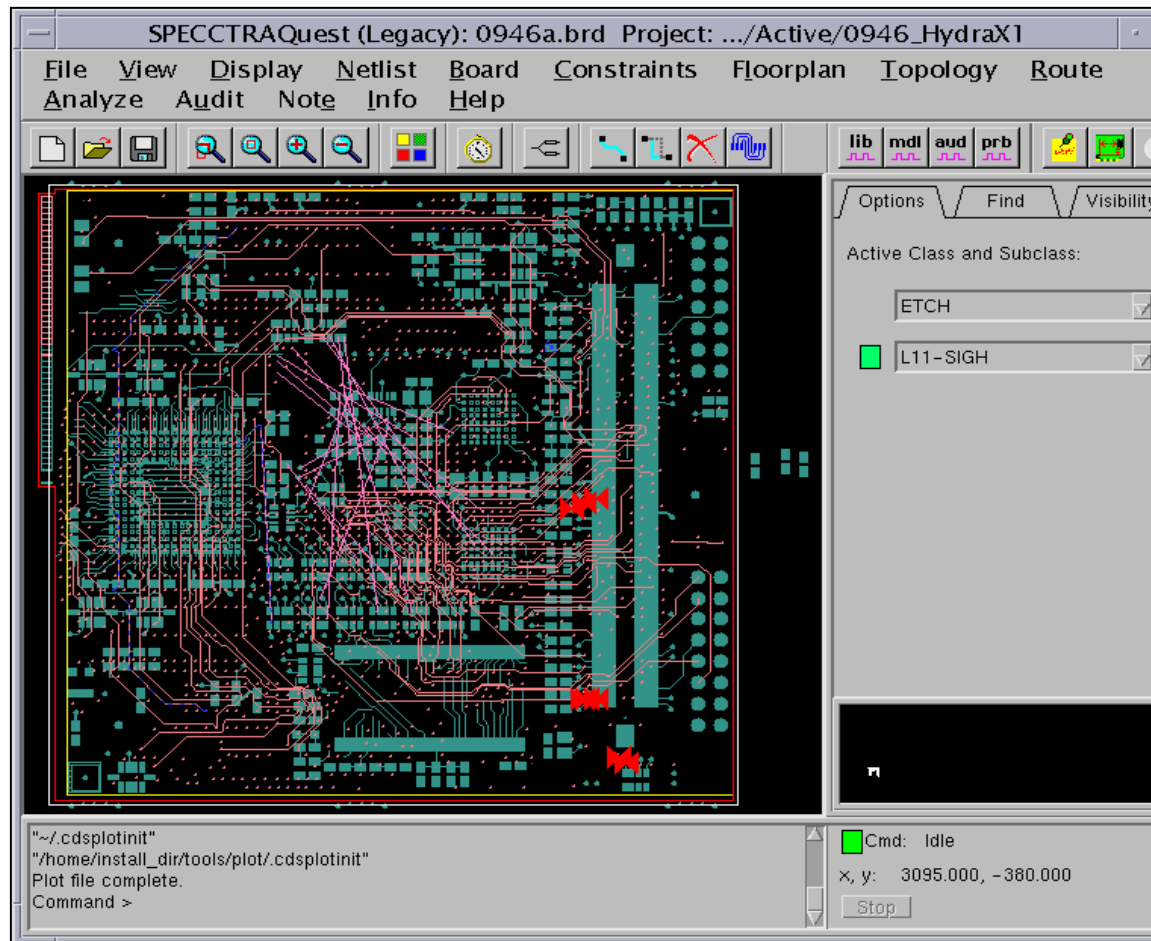
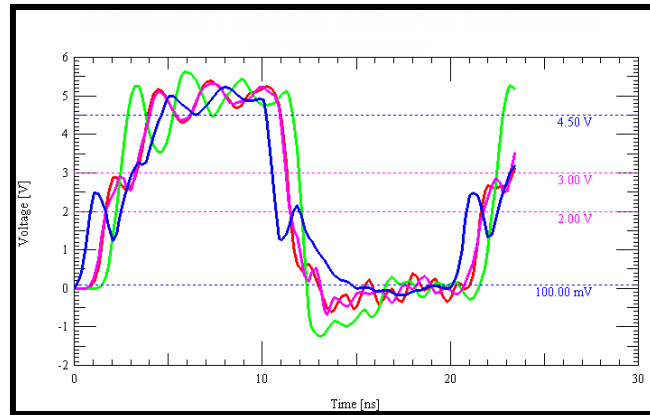
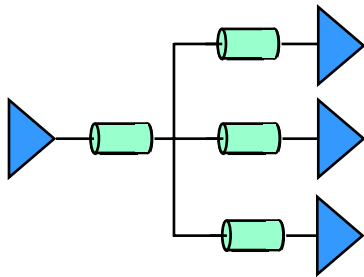


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What Is “High Speed” Design?

- At high speeds, transmission line effects cause receivers to see different signals



- The PCB trace delay must be considered as a set of path-dependent delays

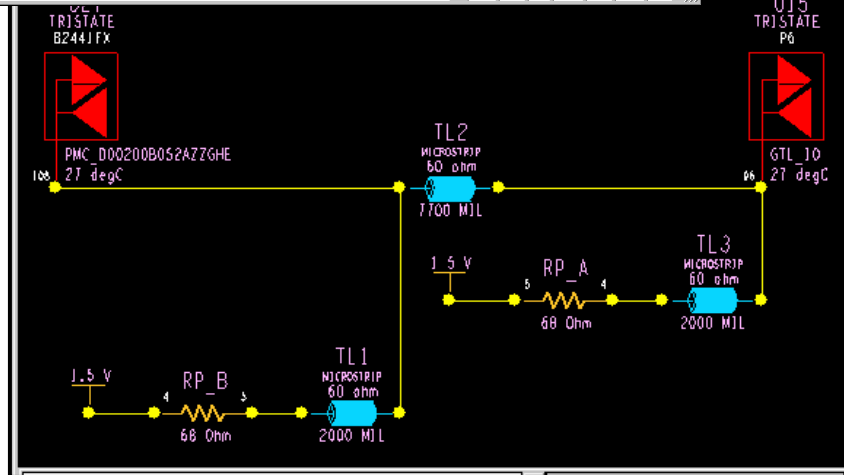
Statistical Design

Microsoft Access - [Sweep_rpt_tab : Table]

FTS-Mode	Driver	Receiver	TL1-Len	TL2-Len	TL3-Len	Sw-Rise	Sw-Fall
Slow/Fast	A U27_108	A U15_96	50	2200	537.5	1.118	0.631
Slow/Fast	A U27_108	A U15_96	50	3575	1025	-0.87	0.88
Slow/Fast	A U27_108	A U15_96	50	6325	1025	-0.346	1.378
Slow/Fast	A U27_108	A U15_96	537.5	2200	1512.5	-1.095	0.643
Slow/Fast	A U27_108	A U15_96	537.5	3575	537.5	-0.869	0.886
Slow/Fast	A U27_108	A U15_96	537.5	4950	2000	-0.588	1.142
Slow/Fast	A U27_108	A U15_96	537.5	6325	1512.5	-0.331	1.389
Slow/Fast	A U27_108	A U15_96	537.5	7700	1025	-0.072	1.627
Slow/Fast	A U27_108	A U15_96	537.5	7700	2000	-0.054	1.632
Slow/Fast	A U27_108	A U15_96	1025	2200	1025	-1.097	0.643
Slow/Fast	A U27_108	A U15_96	1025	3575	1512.5	-0.853	0.895
Slow/Fast	A U27_108	A U15_96	1025	4950	50	-0.617	1.126
Slow/Fast	A U27_108	A U15_96	1025	4950	2000	-0.585	1.145
Slow/Fast	A U27_108	A U15_96	1025	7700	1512.5	-0.059	1.634
Slow/Fast	A U27_108	A U15_96	1512.5	2200	50	-1.101	0.632
Slow/Fast	A U27_108	A U15_96	1512.5	2200	1512.5	-1.086	0.65
Slow/Fast	A U27_108	A U15_96	1512.5	3575	50	-0.867	0.881
Slow/Fast	A U27_108	A U15_96	1512.5	3575	1025	-0.855	0.895
Slow/Fast	A U27_108	A U15_96	1512.5	3575	1512.5	-0.848	0.898

Record: 14 of 208

Datasheet View



- Used to model all possible combinations of conditions the design must operate under
 - Mfg. variances
 - Component speed
 - Trace Impedance
 - Terminator Value
 - Design Variances
 - Segment lengths

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Outline

- What I Present and Why
- Challenges
- Reflections
- The Importance of IC Technology & Modeling
- Working Smart: Objective Measurements, Waveforms, and Setting Priorities
- Additional Sources of Signal Noise
 - Crosstalk
 - Power Bounce
 - EMI/EMC
- Top-Down Design: A New Process for Smart Design
- Enabling Tools

What I Present - and Why

1. The Challenge Ahead

- Speed and complexity are the framework for needing CAE tools to prevent signal integrity and EMI problems

2. Driver Technology Choices and Models

- Speed and driver strength are the prime cause of most electromagnetic effects

3. Screens and Statistical Design: Pass/Fail/Problem Solve

- Complexity of the simulation task drives design methodology

4. The Four Sources of Signal Noise: Reflections, Crosstalk, Ground/Power Bounce and EMI

- Reflections, crosstalk, power integrity and EMI are the four ways of visualizing electromagnetic effects

The Challenge Ahead

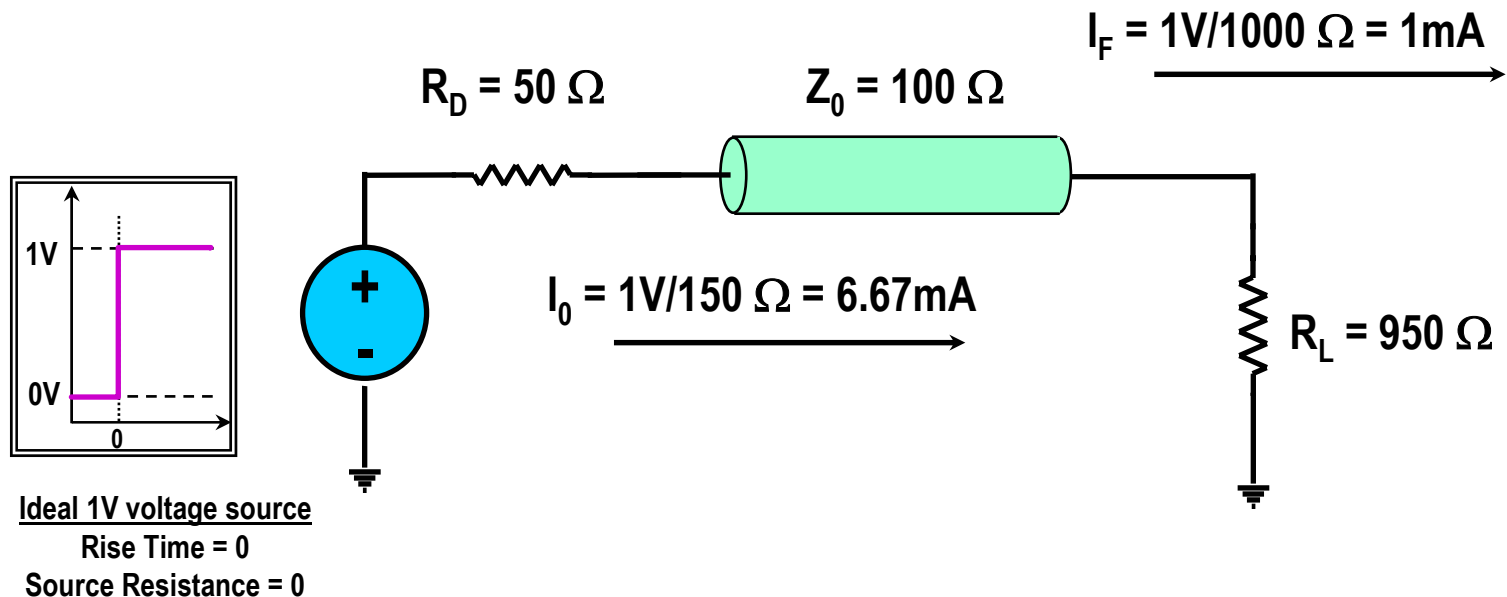
- More speed, faster edge rates
- More functionality and complexity
- More density and crowding
- More EMI and environmental stress
- More price competition and schedule pressure
- Lower voltages with less inherent immunity to noise

Responding to the Challenges

Pathology	Indication (symptom)	Prognosis (untreated)	Therapy
Conducted Tline discontinuities	Reflections	Poor SI = noise on signal, messed up switching logic	Impedance match Lower edge rate Length < $2t_R$
Coupled signal line-line, mostly inductive	Crosstalk	Ditto	Increased space, less parallelism line-line Shielding
Conducted transient voltage sag & ringing	Ground & Power Bounce	Ditto, plus EMI effects	Lower edge rate Lower current Bypass
Conduct, couple & radiate interference / susceptibility	EMI	Regulatory failure, plus SI effects	Treatment per above, plus shield, enclose & source suppress

Impedance Mismatches

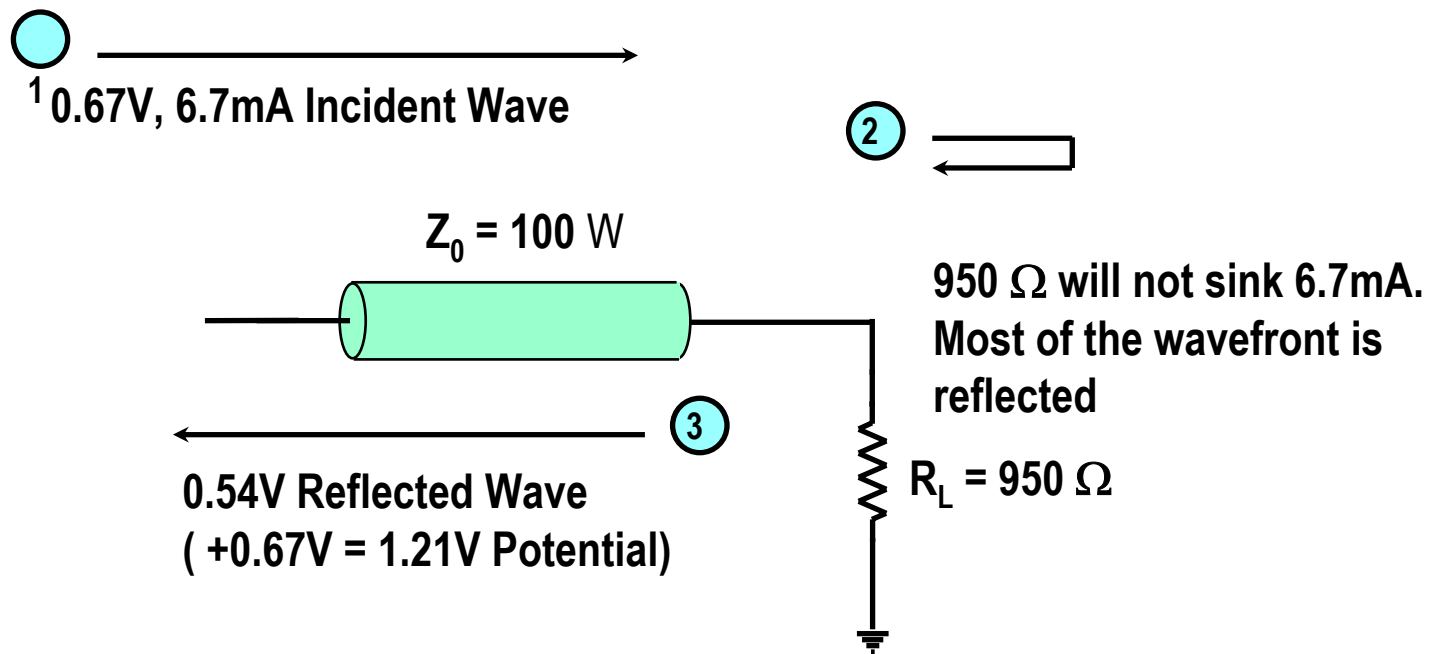
- The transmission line and the load are mismatched, since the initial and steady state currents are quite different



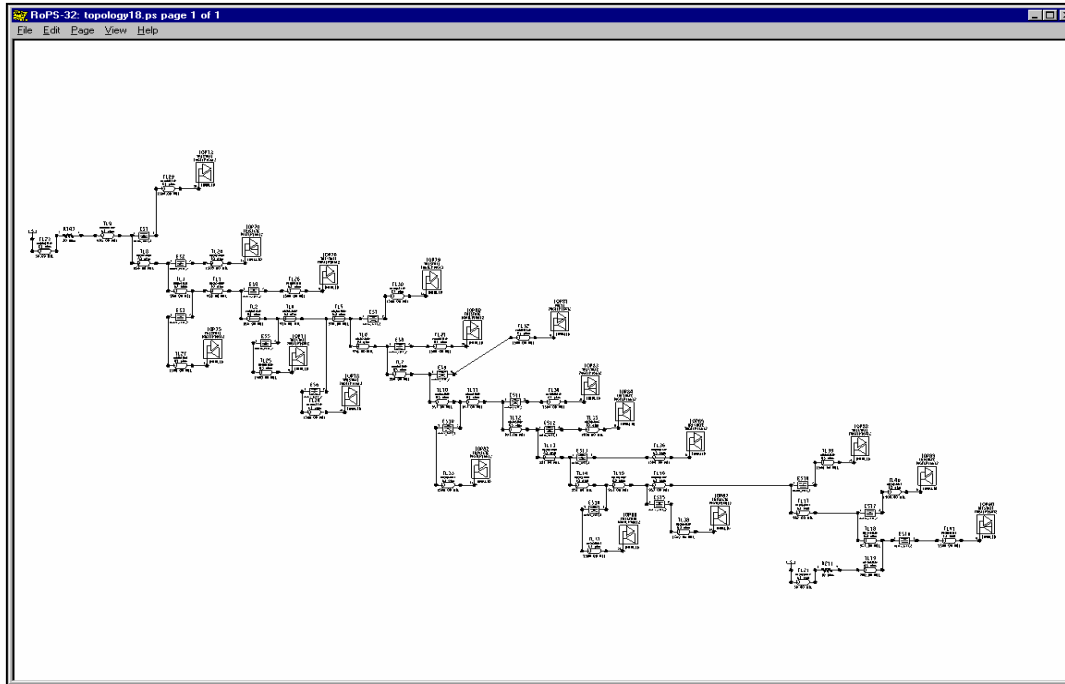
Slide courtesy of Cadence Design Systems used with permission

Reflection

- When the initial wavefront reaches the terminating resistor, most of the voltage is reflected due to the impedance mismatch



For example: A Backplane Bus



“Eye” chart:
standard symbols
for I/Os, sections of
transmission lines,
terminations, etc.

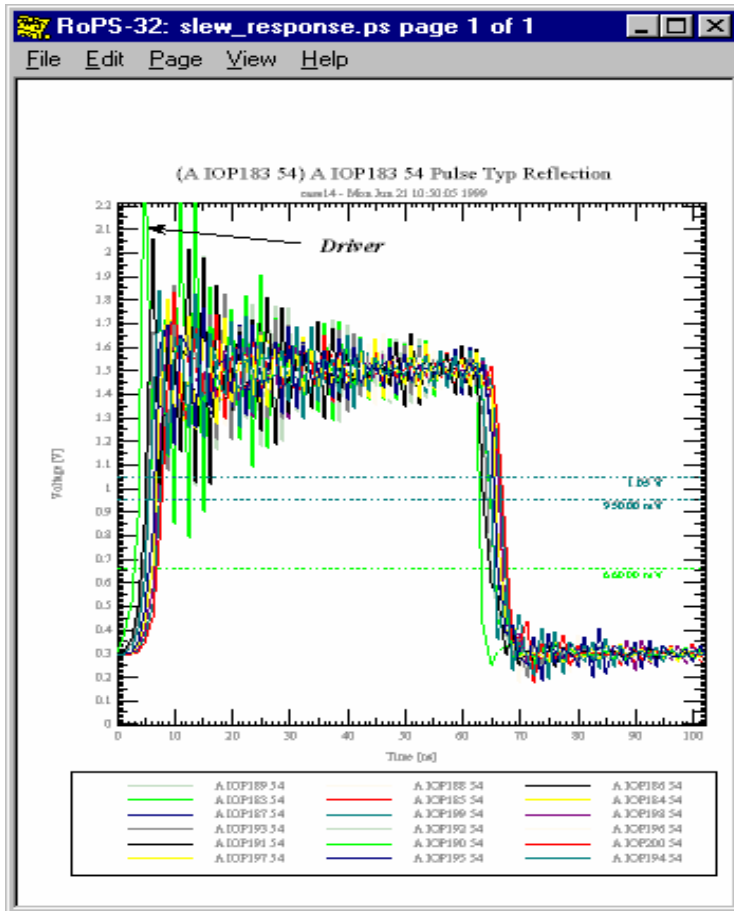
- This is an 18-slot backplane with 1” pitch and 1” stubs at 8mhz.
- The backplane bus, nominal $Z_0 = 63\Omega$, was terminated at each end with a 31Ω pullup resistor for the open-drain GTLP I/Os. Lumped-loaded backplane Z_0 was approximately 25Ω .

Design Challenges

- Speed and complexity interact. Any slot can be the driver position.
- Terminating each stub would add a lot of components in a crowded situation and require a lot more current from the driver.
- How would you design terminations for this backplane bus?
- Transients are still present with RC stub termination. Driver transient currents cause a large spike seen at near neighbors to the driver. What does that spike do to EMI?

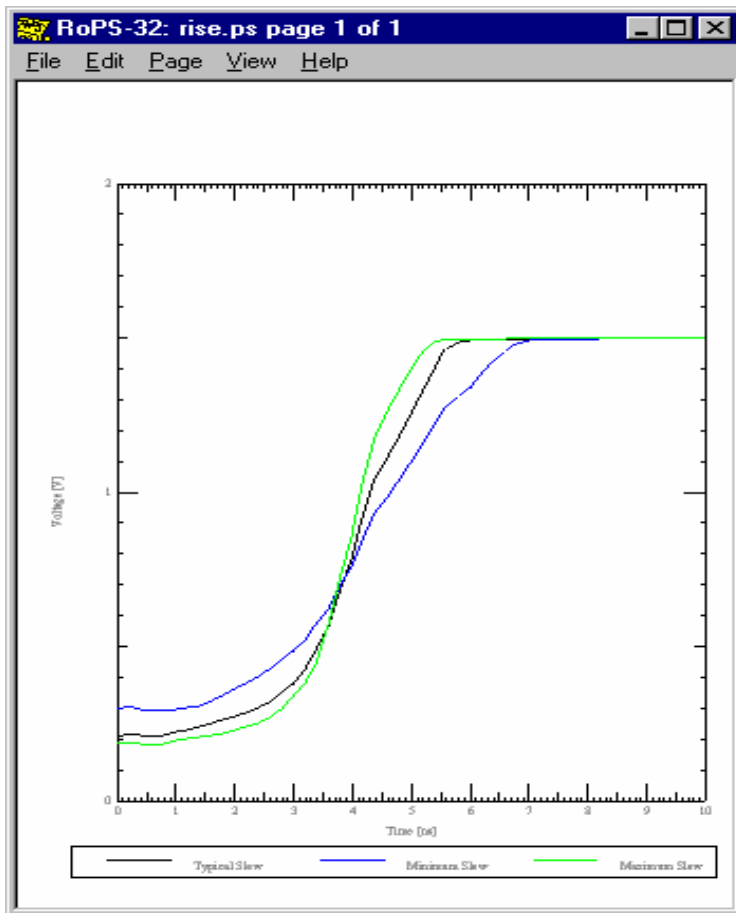
The Impact of IC Technology & Modeling

Driver Technology Choices and Models



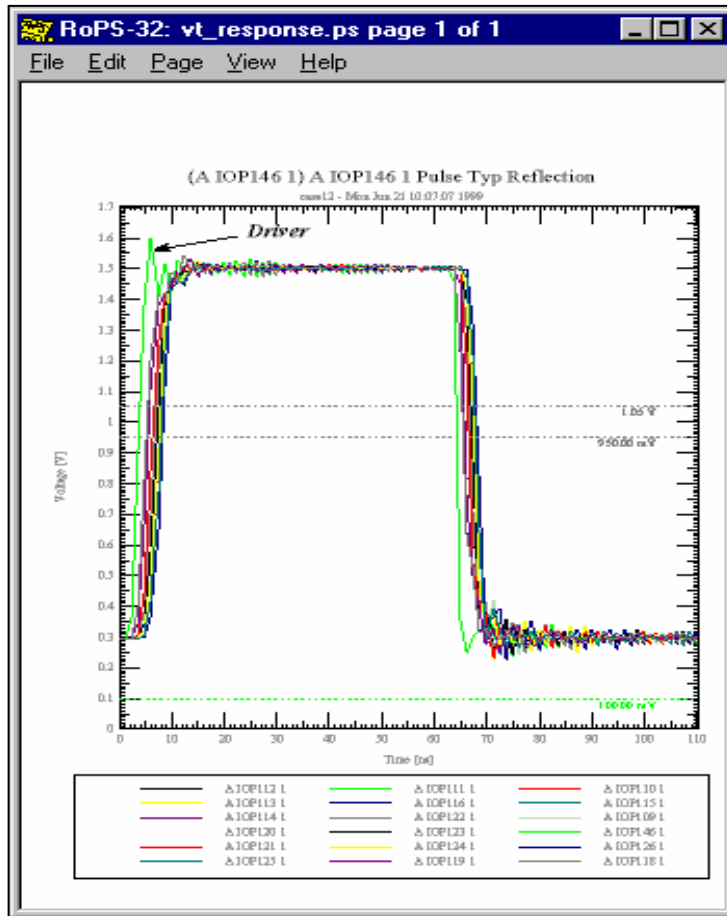
- GTL/GTLP with its soft turnon-turnoff and active (feedback controlled) clamping is expected to perform well in this backplane bus. Why?
- Here is the reflection simulation of the backplane bus as first simulated.
- It's not good enough! - Why?

GTLP: V-T Curve



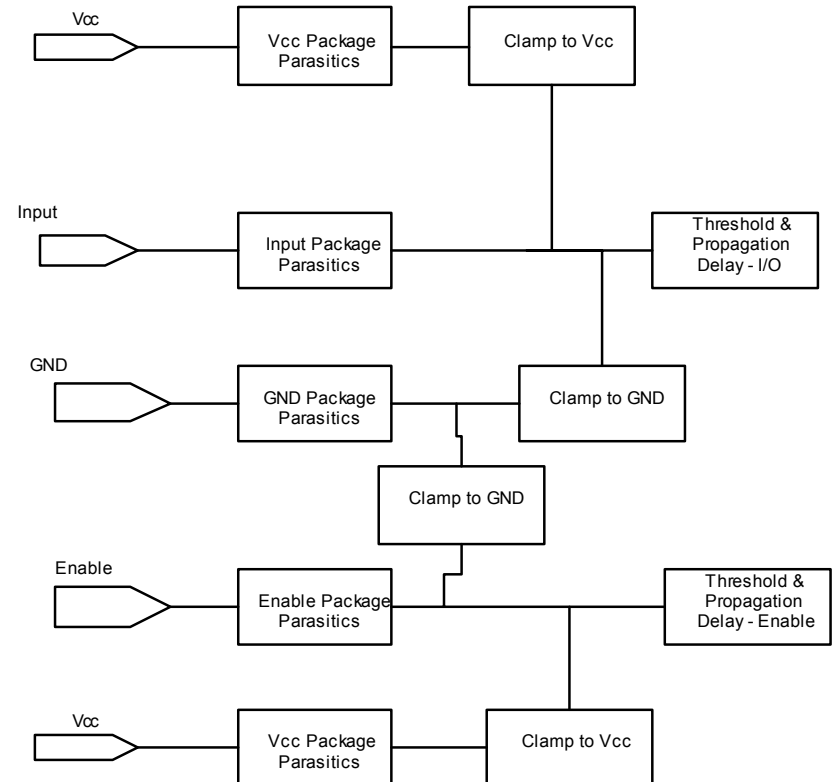
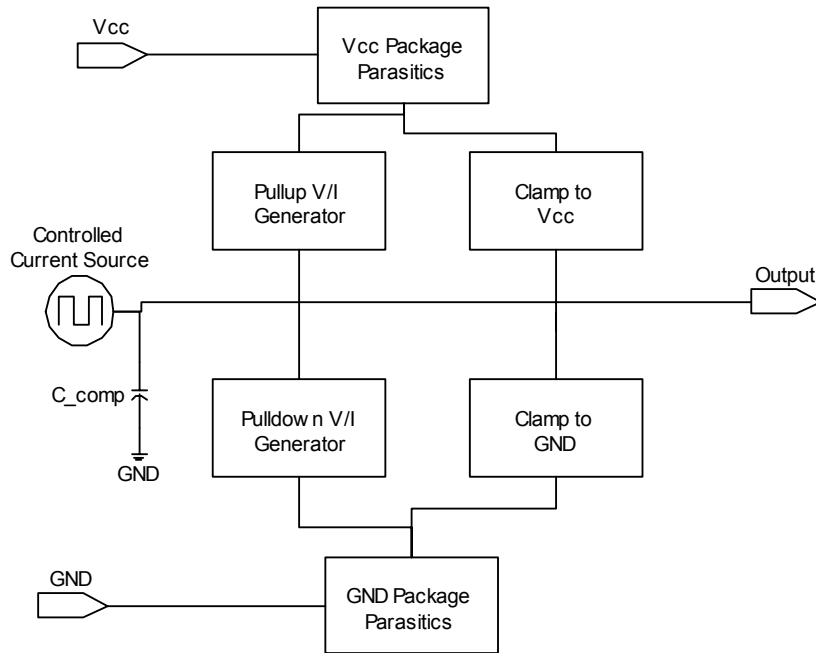
- This is what the rise waveform (V-T curve, min-typ-max) for the selected driver looks like
- A look at the IBIS model file revealed that it had only dV/dt (ramp rate) data

Better Model = Better Results



- This are the results look with a more accurate and sophisticated IBIS model that includes the V-T curve
- We need a blend of technology, topology, and termination choices to meet today's design objectives
- We need to start the SI task at the system / logic design stage
- **What are the timing and noise margin budgets?**
- We can also look at some other technologies like BTL, LVT, etc.

IBIS Model



IBIS Model Page

- <http://www.eigroup.org/ibis/models.htm>
- Links to all model pages known by me



Parse ⇔ The First Quality Screening

```
RUNNING IBISCHK COMMAND: ibischk3 /home/rleventh/Default/xxxxxx/cmos/lv018atm.ibs
IBISCHK3 V3.2.5

Checking lv018atm.ibs for IBIS 2.1 Compatibility...

WARNING - Model 'DS90LV018ATM_ROUTA': TYP AC Rising Endpoints ( 0.01V, 0.94V) not within 0.019V (2%) of ( 0.00V, 1.63V) on
VI curves for 50 Ohms to 0V
WARNING - Model 'DS90LV018ATM_ROUTA': TYP AC Falling Endpoints ( 0.01V, 0.94V) not within 0.019V (2%) of ( 0.00V, 1.63V) on
VI curves for 50 Ohms to 0V

Errors : 0
Warnings: 2

File Passed

END OF IBISCHK COMMAND OUTPUT

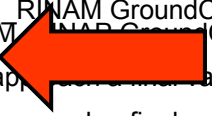
READING IBIS FILE /home/rleventh/Default/National/cmos/lv018atm.ibs

INFO @line 56 --- Completed PackagedDevice DS90LV018ATM
INFO @line 87 --- Completed IbisIOCell DS90LV018ATM_DS90LV018ATM_RINAM
INFO @line 177 --- Completed IbisIOCell DS90LV018ATM_DS90LV018ATM_RINAP
INFO @line 267 --- Completed IbisIOCell DS90LV018ATM_DS90LV018ATM_ROUTA

RUNNING DMLCHECK for lv018atm.dml

WARNING @line 4: DS90LV018ATM_DS90LV018ATM_RINAM GroundClamp: Slope at end is not flat - point added
WARNING @line 89: DS90LV018ATM_DS90LV018ATM_RINAP GroundClamp: Slope at end is not flat - point added
ERROR @line 452: TVCurve must start at time zero
WARNING @line 452: TVCurve should asymptotically approach a final value - point added
ERROR @line 180: TVCurve must start at time zero
WARNING @line 180: TVCurve should asymptotically approach a final value - point added

Translation failed due to DMLCHECK errors.
Output saved as lv018atm.dml.txt for examination.
```



An untypical conversion report (it is short). But, it involves regenerating the T-V curve. It's too labor-intensive to do, so send it back to the supplier.

Common Mistakes (cont.)

- **Syntax errors of all sorts**

For example: Tab characters following keywords, lines longer than 80 ASCII characters, non-ASCII characters, (/) \ % @ # * etc., etc. Data item names too many characters long. Missing keywords and data items. Literal (actual) keywords inserted in the text of un-commented-out notes. File names that are different than the [File Name] keyword. Etc.

Only spaces and underbars "_" are allowed in names.

Syntax errors in supplied IBIS models are so common as to hardly bear mentioning!

Correction: Use the latest version of the IBIS Standard, the IBIS GoldenParser (downloaded from their website) and the "IBIS Model Syntax Guide" to diagnose and fix the problem.

Otherwise, have the IBIS model supplier send you a corrected file.

- **More Info At:**

<http://www.eda.org/pub/ibis/training/3com-docs/E0173.doc> page 55

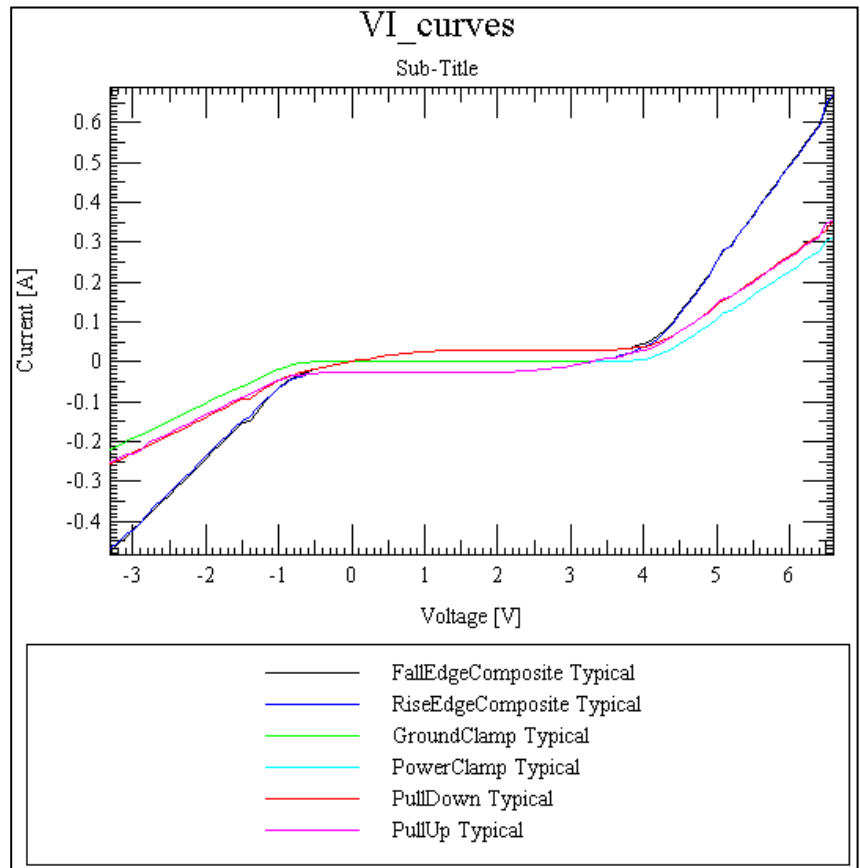
Love Your Parser!



- The Parser is your friend!
- Learn to Love it!

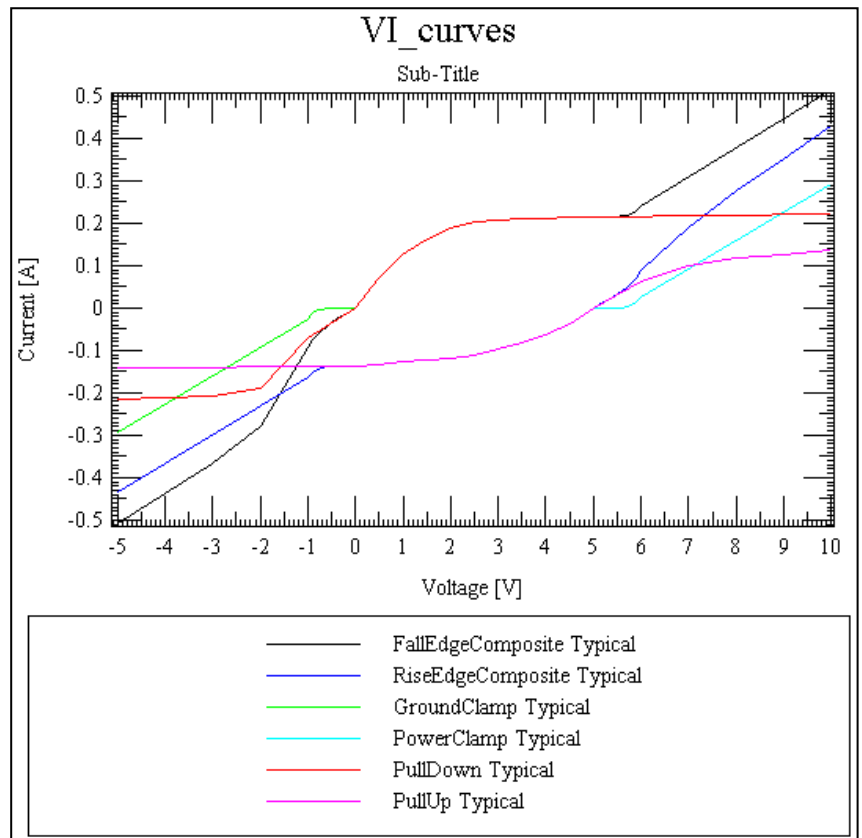
Models and Reality Checks: An Example:

- Here is an example of something that doesn't check out - the dark blue composite VI curve goes up (down) at twice the rate of its power (ground) clamp curve
- The IBIS data exchange format calls for storing the VI data in 4 separate tables

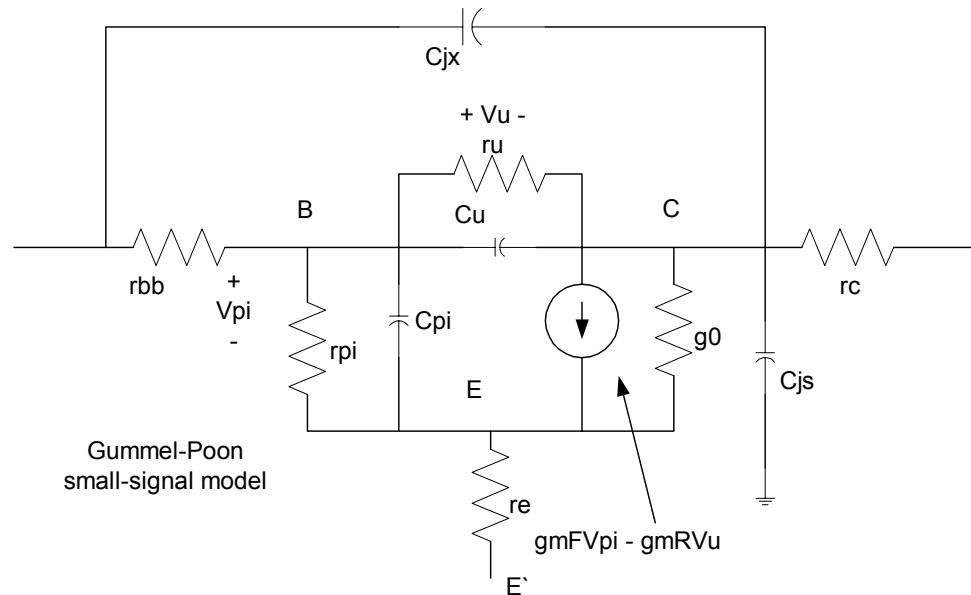


In this example Reality = data stored correctly:

- The four components of properly stored data are separate VI curves for Pullup, Pulldown, Power Clamp and Ground Clamp
- This time the clamps don't get double counted because that V-I data was not properly decomposed and stored to begin with



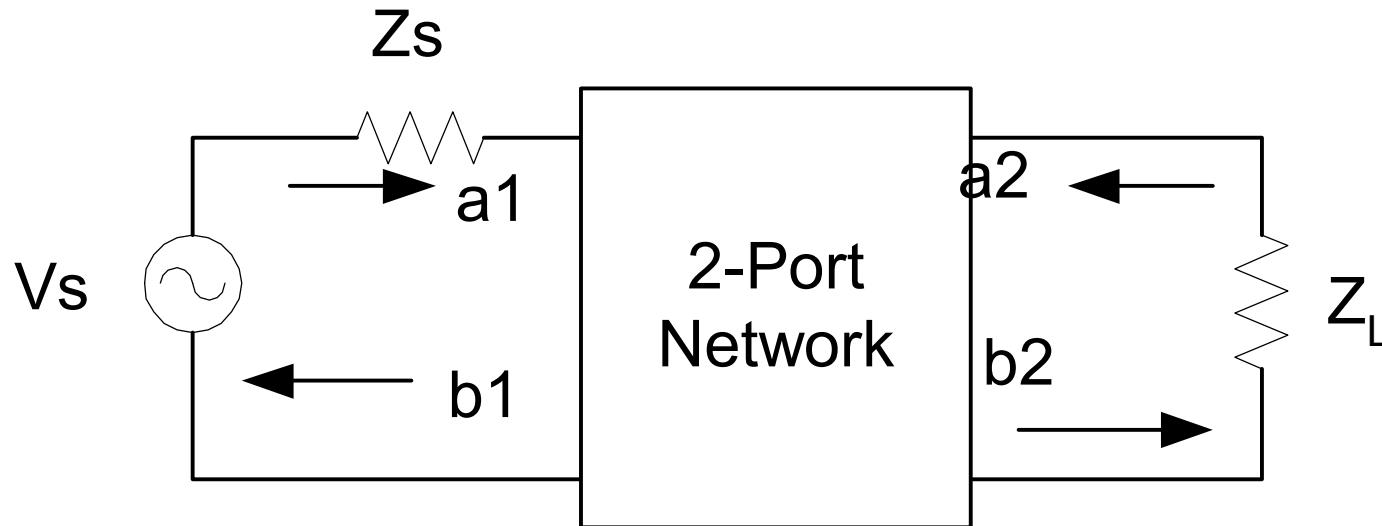
SPICE



- * Model Generated by MODPEX **Copyright (c) Symmetry Design Systems All Rights Reserved Model generated on Apr 22, 96 .MODEL 2N3904 npn

• IS=6.9716e-14 BF=545.416 NF=1.09328 VAF=10 IKF=0.0228393
 ISE=5.71808e-12 NE=1.88204 BR=4.70256 NR=1.3912 VAR=2.31769
 IKR=0.074093 ISC=5.71808e-12 NC=1.36259 RB=1.733 IRB=1.12054
 RBM=0.876202 RE=0.356192 RC=1.78096 XTB=0.1 XTI=1 EG=1.05
 CJE=4.47982e-12 VJE=0.4 MJE=0.240345 TF=4e-10 XTF=1.5 VTF=1 ITF=1
 CJC=3.76637e-12 VJC=0.4 MJC=0.241382 XCJC=0.8 FC=0.533333 CJS=0
 VJS=0.75 MJS=0.5 TR=3.77901e-05 PTF=0 KF=0 AF=1

Scattering Parameter



- ! Vcc = 5.0V
- # HZ S MA R 50
- 1.00000E+008 7.12835E-001 -3.63994E+001 1.27654E+001 -1.15192E+002 3.47731E-003
-1.02163E+002 9.41197E-001 -8.77695E+000
- 1.29000E+008 6.77515E-001 -3.80355E+001 1.26185E+001 -1.24682E+002 2.38669E-003
-1.02781E+002 9.14716E-001 -7.94114E+000
- 1.58000E+008 6.31758E-001 -4.12172E+001 1.28985E+001 -1.36511E+002 6.96522E-004
-7.01082E+001 8.84407E-001 -6.04719E+000

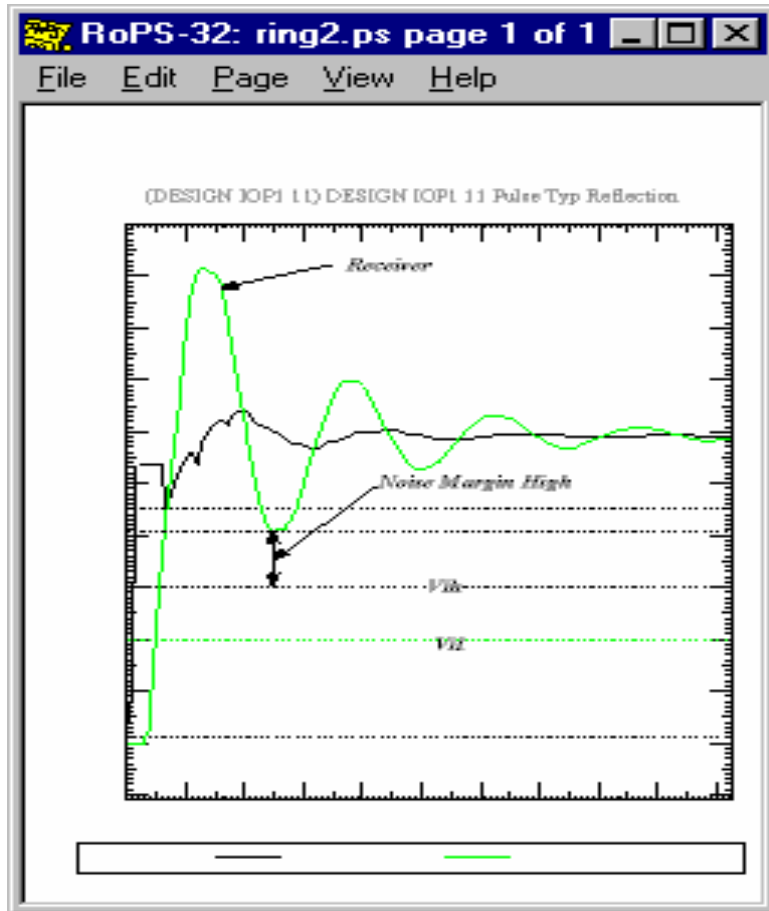
Technology - Comparisons

Basic Tech.	Type	t_r (nS)	Bandwidth (MHz)	$1/2 \lambda$ (inch) stripline
TTL	LS	6	53	16.67
	ALS	3	106	8.33
	FAST	2	159	5.55
CMOS	MG	50	6.4	139
	HC	4	79.5	11.11
	FACT	2	159	5.55
ECL	10H	1	318	2.78
	100K	.7	455	1.94
	ECLinPS	.5	637	1.39
GaAs		.2	1590	0.56

Waveforms Versus Measures of SI

- Time domain waveforms (and, frequency domain spectral density/power plots) are great for diagnostics and design. But:
- Measurements of switching parameters (First Switch, Final Settle, etc.) arranged in tables, and sorted by magnitude must be used to **prioritize** a multi-net, multi-I/O buffer board so that you can focus on what is important.
- Some of these SI parameters are presented next:

Noise Margin

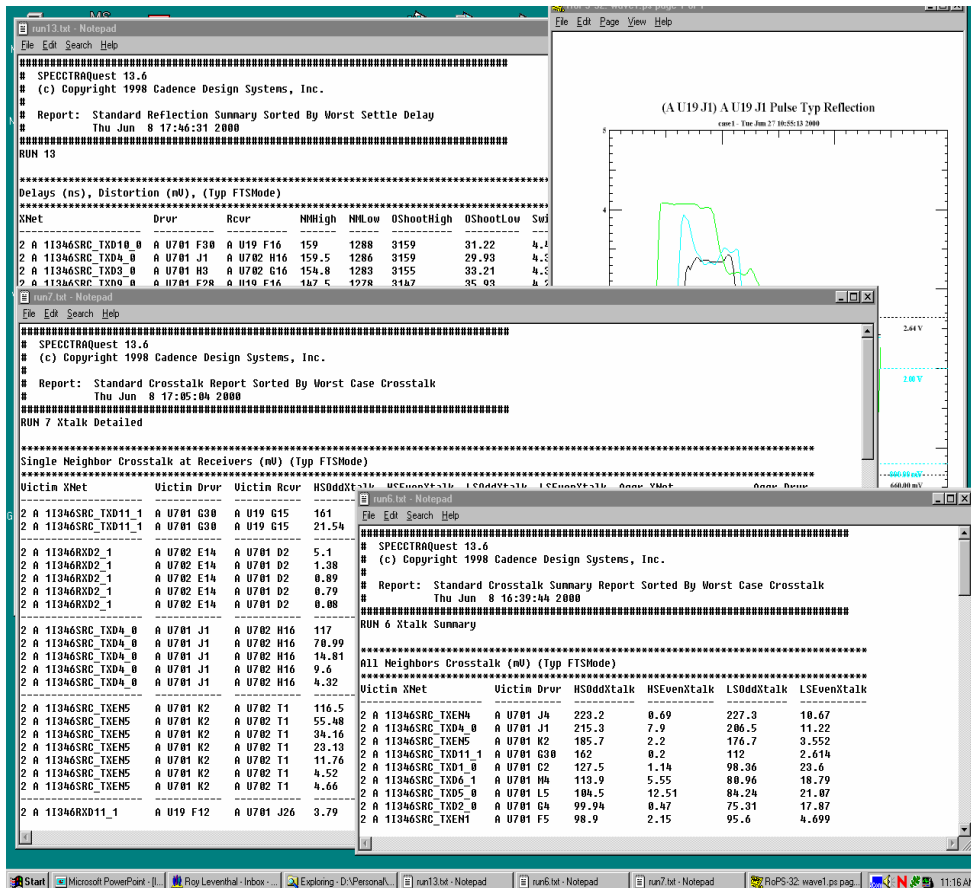


- Noise margin = margin of signal amplitude safety (avoiding switching jitter or bounce) between a receiver's input and the input's switching threshold
- The input thresholds shown, V_{il} and V_{ih} , are the *population's* spread in values for a population of receiver devices
- The ***inherent*** noise margins, NM, of a technology are:
 - $NM_{high} = V_{oh} - V_{ih}$
 - $NM_{low} = V_{il} - V_{ol}$

Noise and Timing

- The most important SI question for a digital product is:
Will the logic work?
 - This translates to: can I meet my **timing budget** with enough **noise margin** to do it reliably?
 - First switch, overshoot and crosstalk are informative of the signal integrity and noise margins of a design
 - But, the measurements and parameters that come from signal integrity simulations that directly tell us about timing budgets are final settle, t_{pd} and clock skew

Measurements & Statistical Design: pass/fail/problem solve



- Whole board scans at a summary report level first
- Detailed simulations on possible problem nets next
- Then, individual net problem solving with waveforms, topology and model manipulation
- Typical board:
 - 1449 Components
 - 2138 Nets
 - 27 Layers (including dielectrics)

Additional Sources of Signal Noise:

Crosstalk - All

```

• # SPECCTRAQuest 13.5
• # (c) Copyright 1998 Cadence Design Systems, Inc.
• # Report: Standard Crosstalk Summary Report Sorted By Worst Case Crosstalk
• # Tue Sep 14 22:35:37 1999
• *****
• All Neighbors Crosstalk (mV) (Typical FTSMODE)
• *****
• Victim XNet                Victim Drvr  HSOddXtalk  HSEvenXtalk  LSODdXtalk  LSEvenXtalk
• -----
• 3 E PLUS_FIVE_EN_N         E U56 40    1059              NA              1123              NA
• 2 E DP0_TDI                 E U20 17    1022              NA              863.9             NA
• 1 E PC_RESET_OUT_N   . . .
• . . .
• 2 E BM_PADR13              E U60 C10    112.3              NA              106.3             NA
• 3 E BMCI_PDATA26          E U50 57     112.3              NA              91.03             NA
• 1 E P_AD15                 E J1 D33     110.7              NA              111.6             NA
• 2 E BM_MWEB_N              E U60 AC16    109.6              NA              85.96             NA
• 1 E PPCI_AD10              E U41 115     NA . . .

```

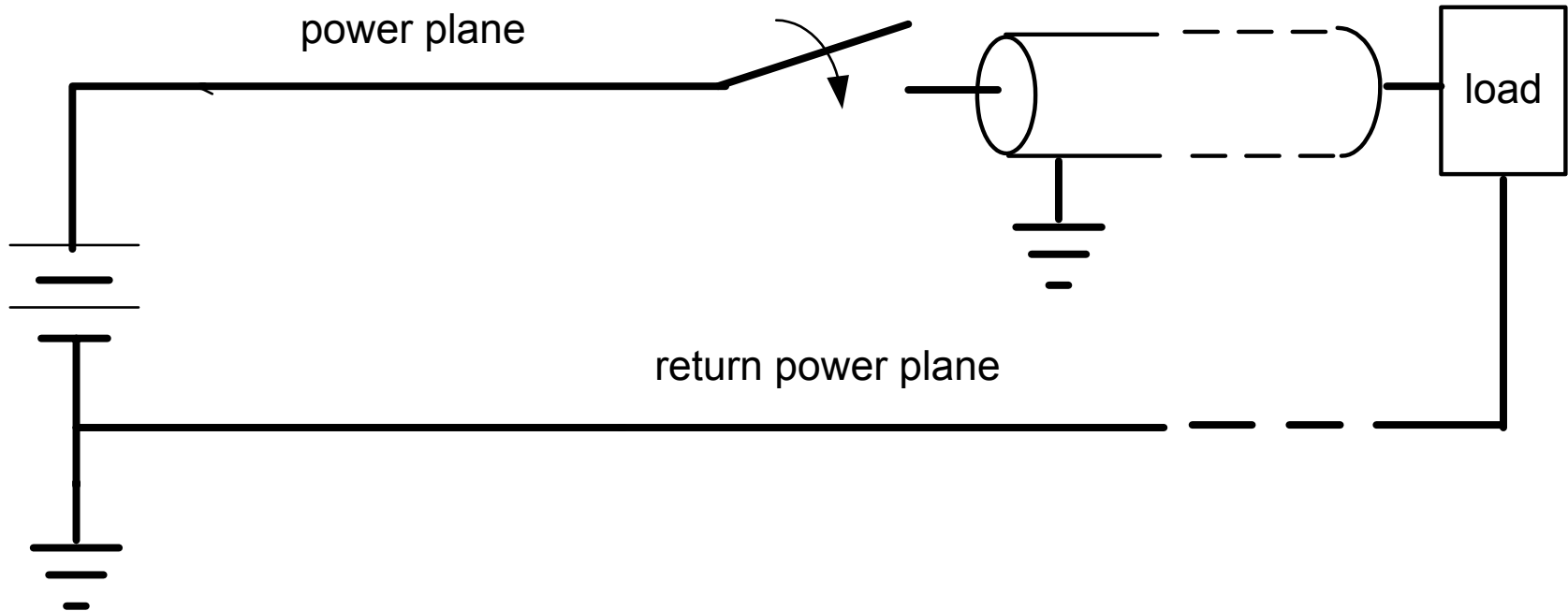
Crosstalk-Each: Diagnostics

```

• # SPECCTRAQuest 13.5
• # (c) Copyright 1998 Cadence Design Systems, Inc.
• # Report: Standard Crosstalk Report Sorted By Worst Case Crosstalk
• # Wed Sep 15 11:14:56 1999
• *****
• Single Neighbor Crosstalk at Receivers (mV) (Typ FTSMODE)
• *****
• Victim XNet      Victim Drvr  Victim Rcvr  HSOddXtalk  HSEvenXtalk  LSOddXtalk  LSEvenXtalk  Aggr XNet      Aggr Drvr
• -----
• 1 E PC_RESET_OUT_N E U56 2      E U64 4      942          NA           704.6        NA           2 E 25N291      E U64 8
• 1 E PC_RESET_OUT_N E U56 2      E U64 4      219          NA           144.6        NA           1 E TSI_RX_HWY4  E U59 H4
• 1 E PC_RESET_OUT_N E U56 2      E U64 4      87.92        NA           72.58        NA           1 E NIC_TX_HWY2  E U18 30
• -----
• 3 E PLUS_FIVE_EN_N E U56 40     E U2 4       680.7        NA           578.5        NA           2 E SPCI_SERR_N  E U12 40
• 3 E PLUS_FIVE_EN_N E U56 40     E U2 4       377.3        NA           317          NA           1 E LPB_AD27     E U8 17
• 3 E PLUS_FIVE_EN_N E U56 40     E U2 4       260.4        NA           260.4        NA           1 E SPCI_C_BE3_N E U41 25
• 3 E PLUS_FIVE_EN_N E U56 40     E U2 4       2            NA           1.689        NA           9 E 21N964       E U58 J2
• -----
• 1 E NIC_TX_HWY2     E U18 30     E U50 2      485.6        NA           410.3        NA           2 E 25N291      E U64 8
• 1 E NIC_TX_HWY2     E U18 30     E U50 2      182.6        NA           148.5        NA           1 E P_AD22       E U11 11

```


Power Bounce (& Ground) Basics



- Voltage bounce on ground and power is a major EMI headache
- Power/ground planes can be modeled, simulated and designed for good power distribution. Cadence has a PowerIntegrity® product.

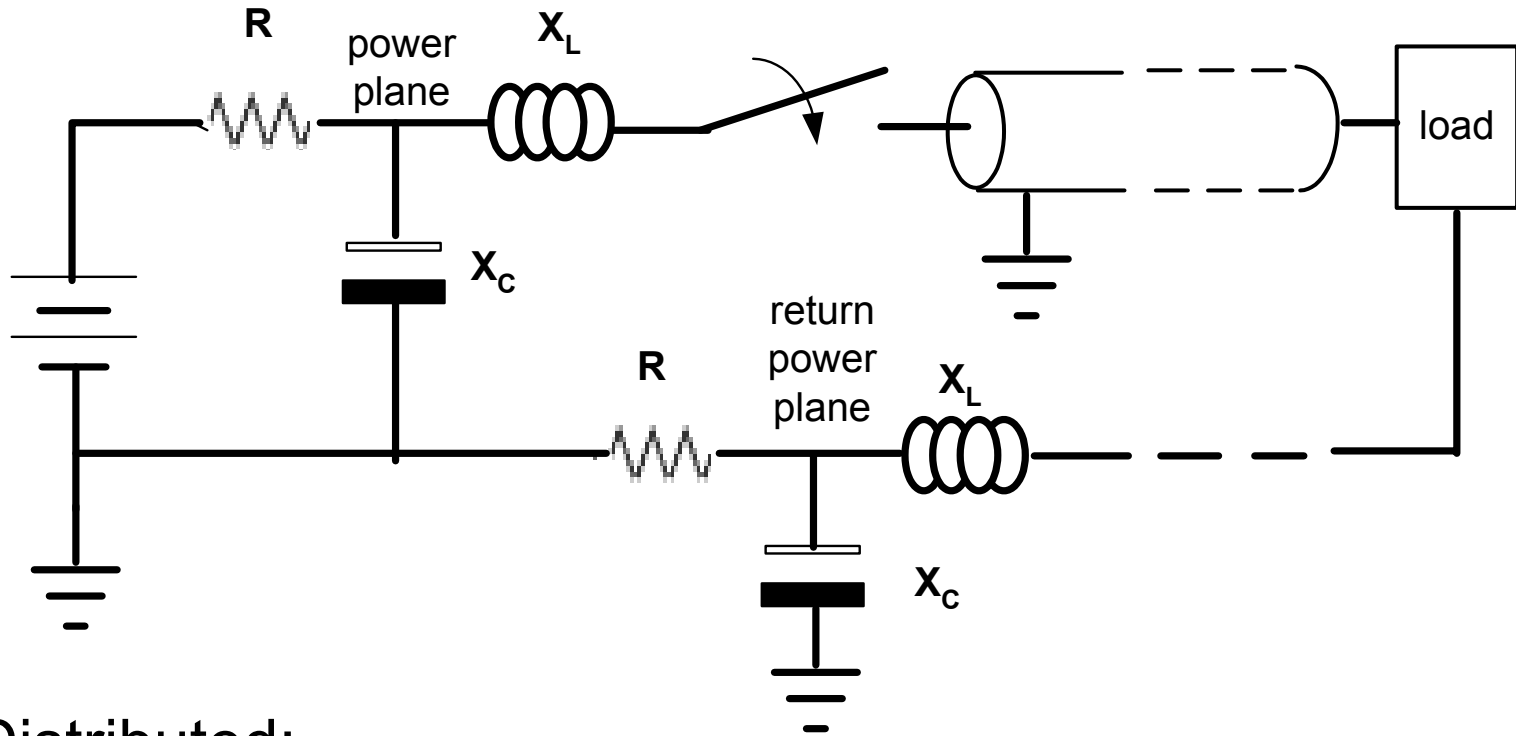
Power Bounce (& Ground) Basics (cont.)

Power Delivery Requirements

Year	Voltage (Volts)	Power (Watts)	Current (Amps)	Z _{target} (m-Ohms)	Frequency (MHz)
1990	5	5	1	250	16
1993	3.3	10	3	54	66
1996	2.5	30	12	10	200
1999	1.8	90	50	1.8	600
2002	1.2	180	150	0.4	1200

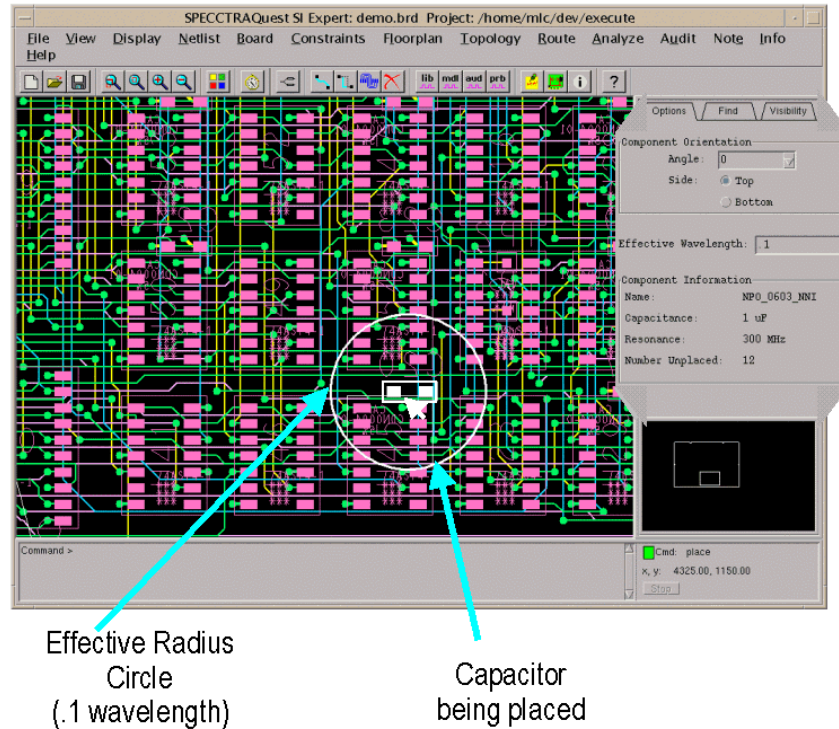
- Chip power supply voltages are decreasing
 - Maximum allowable supply ripple decreases accordingly
- Modern CMOS devices continue to dissipate more and more power
 - The instantaneous switching current required is enormous!

Power Bounce (& Ground) Basics (cont.)



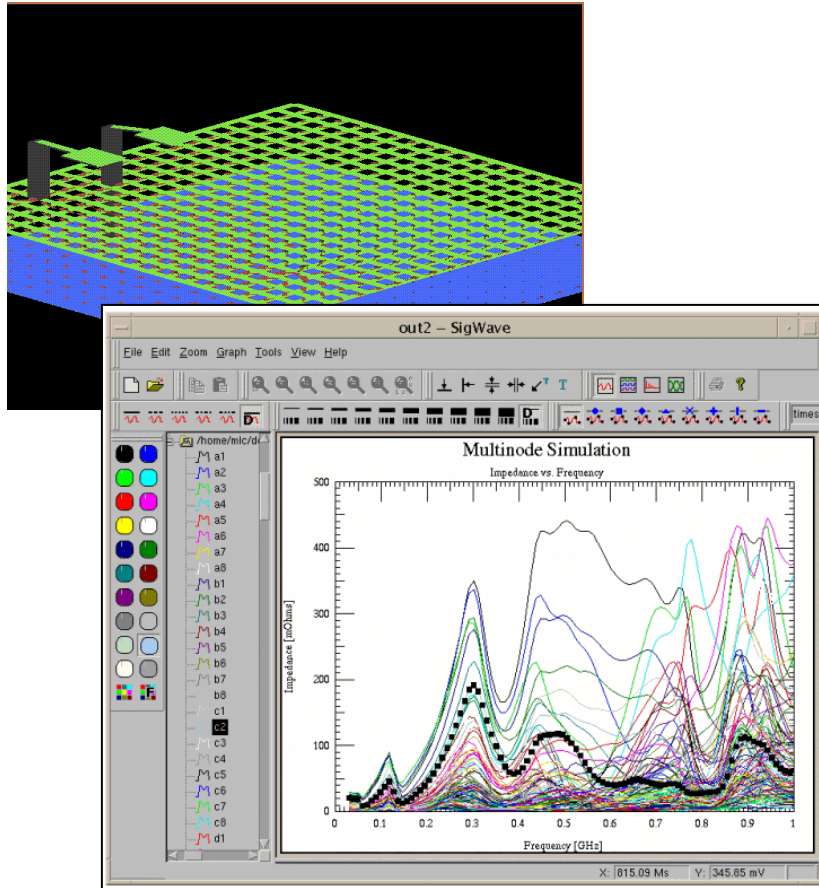
- Distributed:
 $v_R = iR$, $v_C = iX_C$, $v_L = iX_L$, $X_C = -j/2\pi fC$, $X_L = j2\pi fL$
- Switch characteristics: V-I & V-T curves, pin parasitics, etc. See the IBIS Model.

Device Placement for Decoupling Capacitors



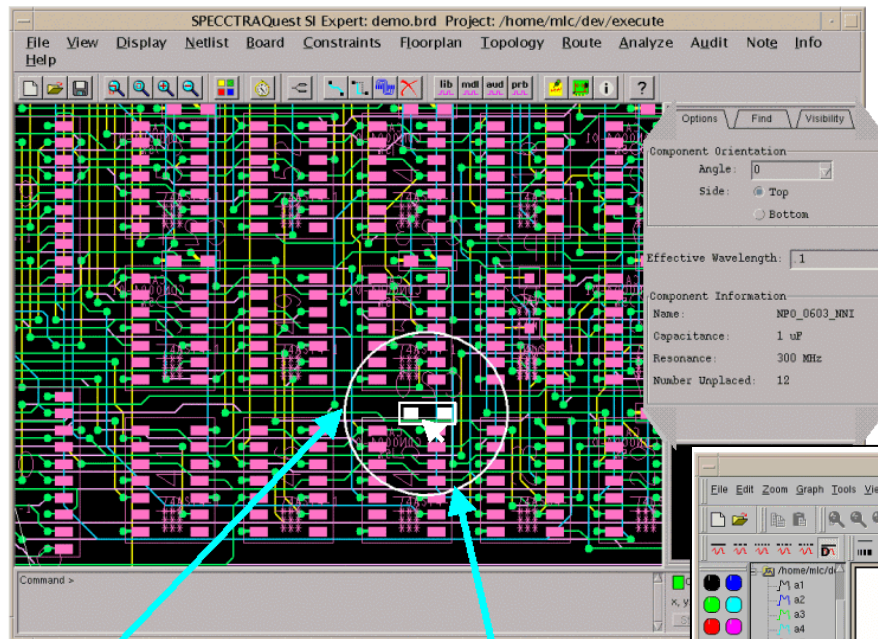
- Capacitors can be selected from the decoupling “menu” and placed into the design
- The effective decoupling radius is automatically displayed as the capacitor is positioned

Analyze PDS Behavior



- Frequency-domain analysis engine meshes power planes and predicts $Z_{(f)}$ at different points on the power plane
- $Z_{(f)}$ plots can be superimposed to quickly locate problem areas in the power delivery system

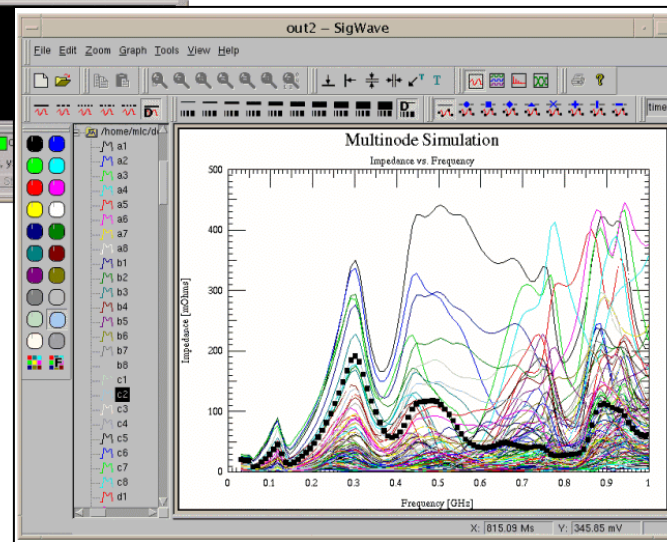
Refining Capacitor Placement



Effective Radius
Circle
(.1 wavelength)

Capacitor
being placed

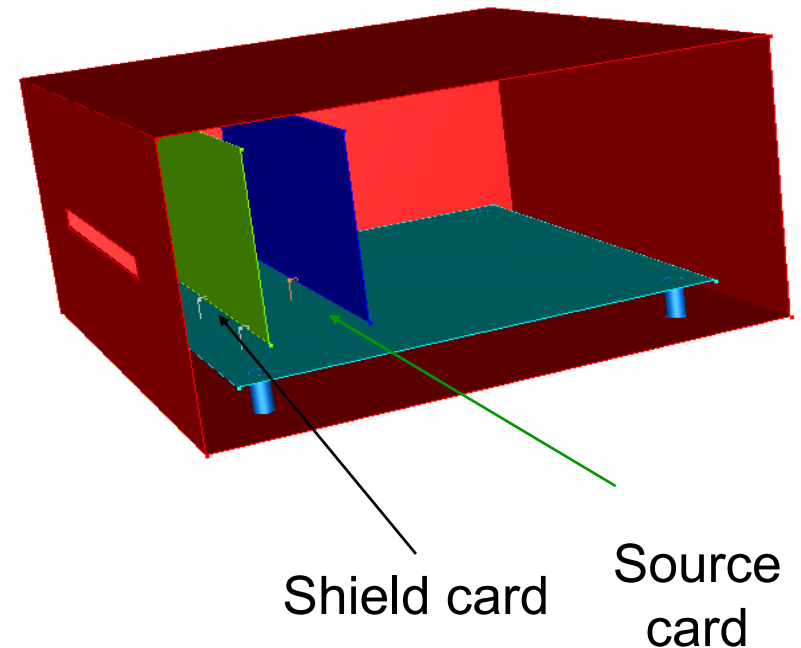
- Designers continue to adjust capacitor selection & placement until performance of the PDS is acceptable



EMI/EMC

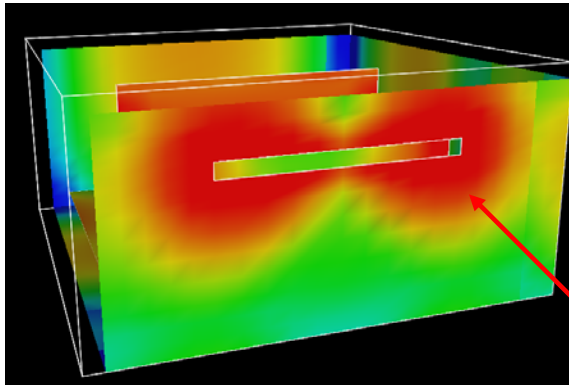
IEEE - TC9 Challenge Problem: System Grounding

- Metal box size 30x15x30 cm
- Front slot 15x1 cm
- Main board grounded to chassis in 4 corners using metal standoffs
- Source card is driven with 1V source (50 Ohms impedance)
- Shield card connected to main board using 3 ground wires

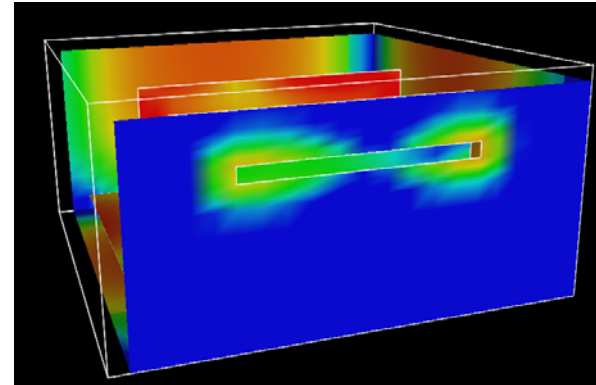


External Surface Current

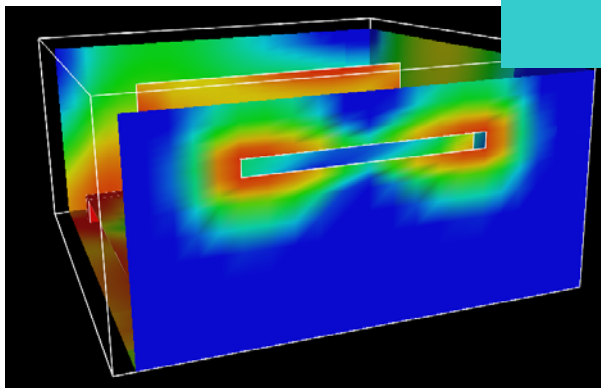
Baseline



Ground Pins Only

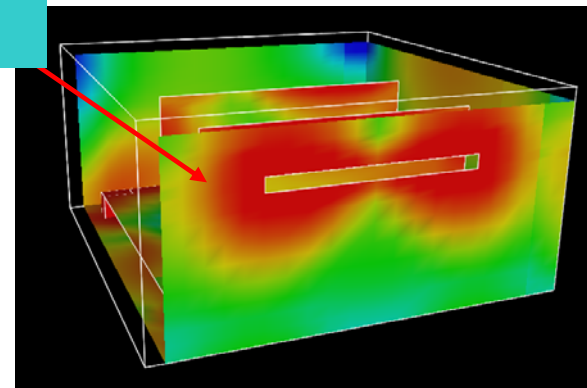


Standoffs Only



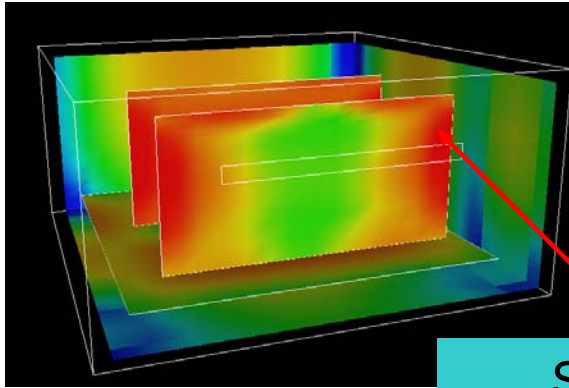
Strong Coupling
to Slot
Why???

Pins and Standoffs

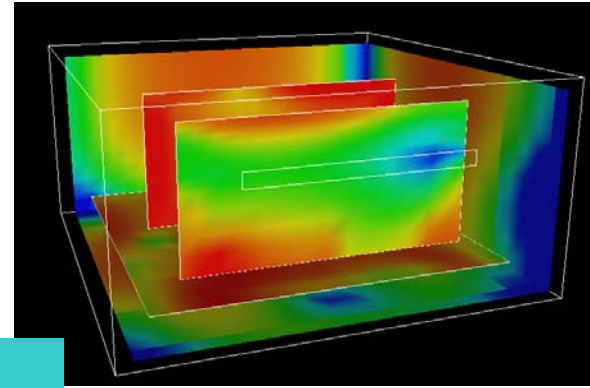


Internal Surface Current

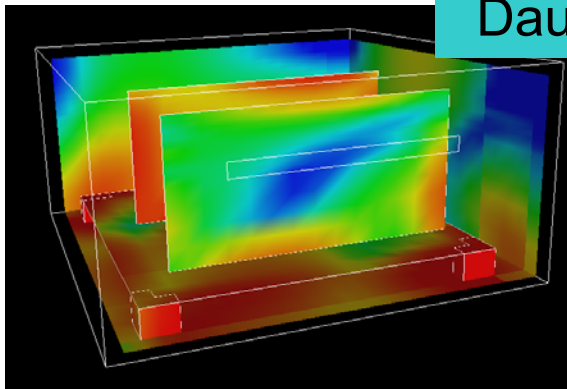
Baseline



Ground Pins Only

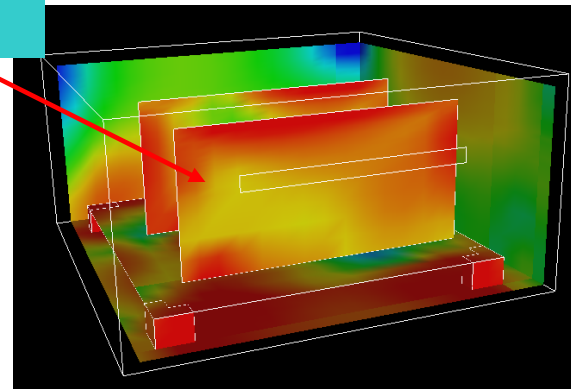


Standoffs Only



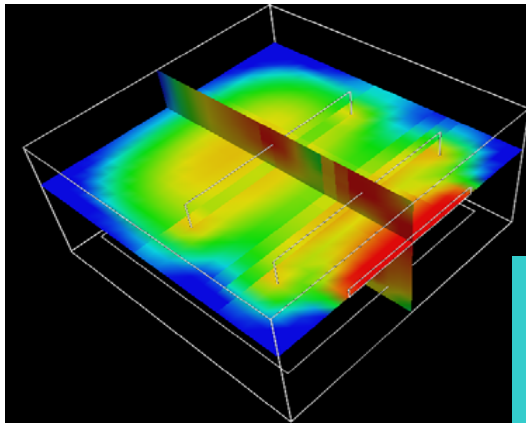
Stronger
Currents on
Daughter Card

Pins and Standoffs

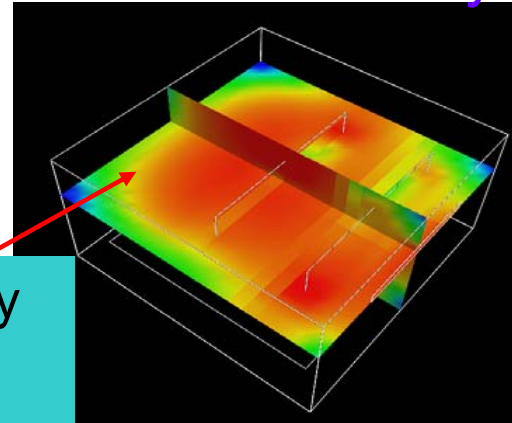


Internal Fields

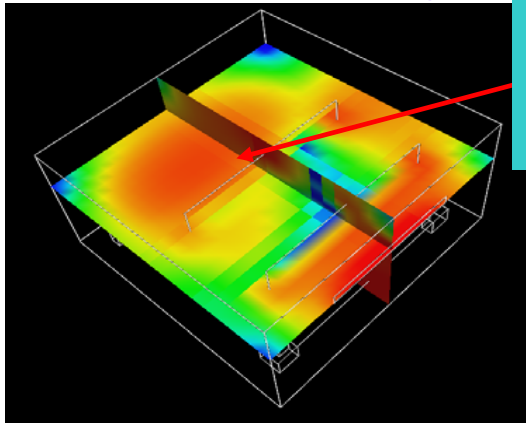
Baseline



Ground Pins Only

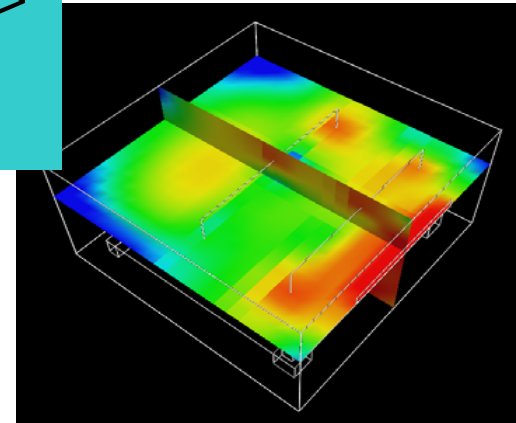


Standoffs Only



More Energy
Stored in
Interior
Resonance =>
Less
Radiation!!

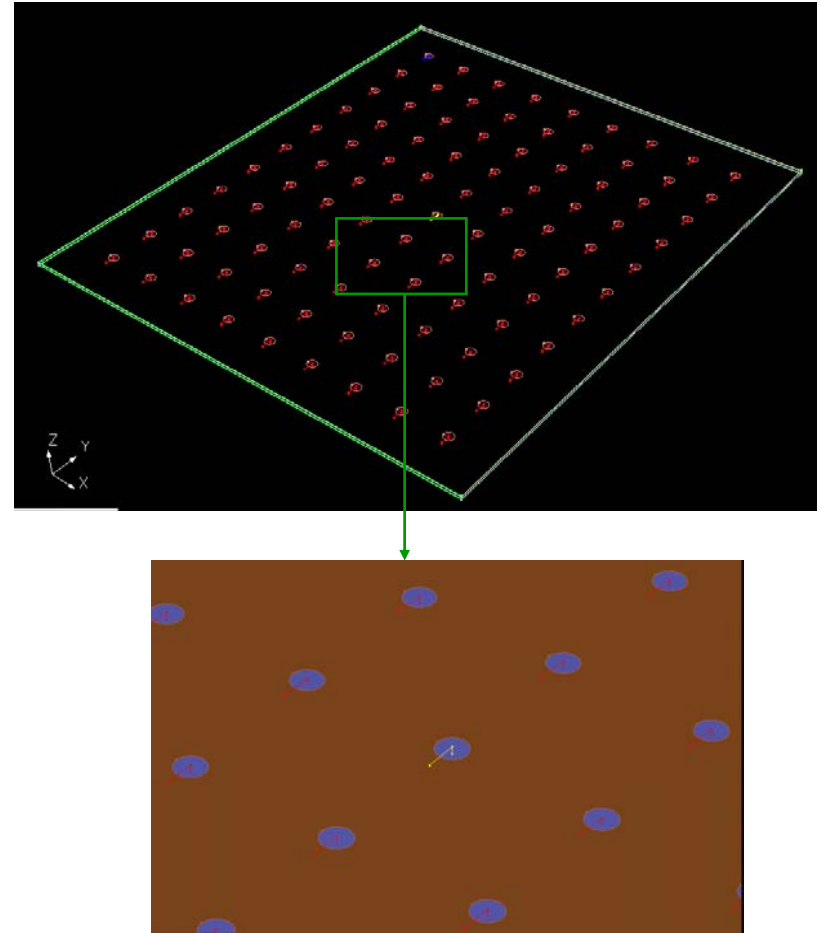
Pins and Standoffs



IEEE - TC9 Challenge Problem

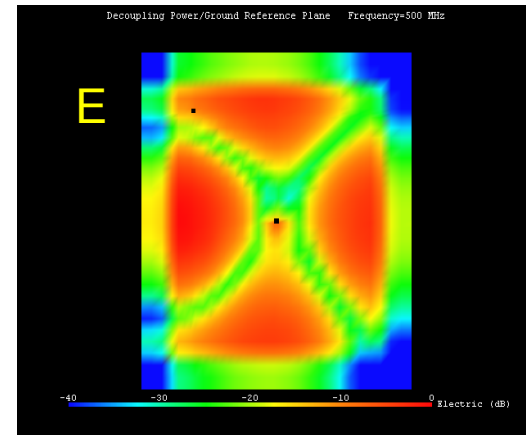
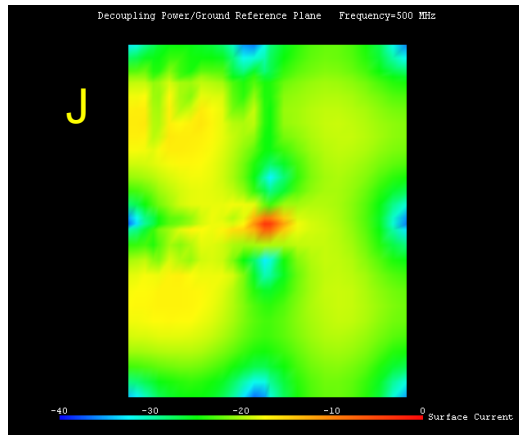
Power / Ground Decoupling

- Test board is a 4-layer board with 2 solid planes in inner layers separated by 40 mils dielectric FR4
- Plane size is 10" x 12"
- 99 decoupling capacitors located on a 1" pitch across the board
- Decoupling capacitors are 0.01mF with a series resistance of 50 mOhms and an inductance of 2nH.
- Lumped series L-C-R circuit is connected to a via-wire located between the power and ground plane

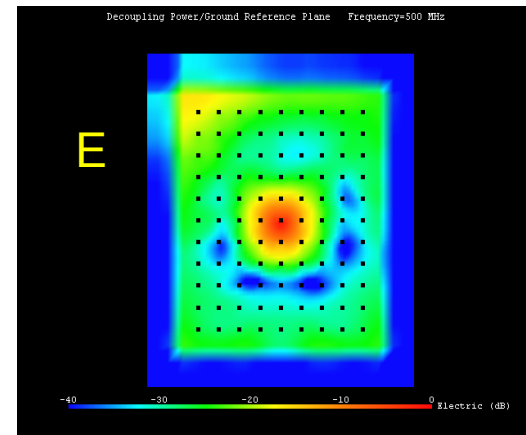
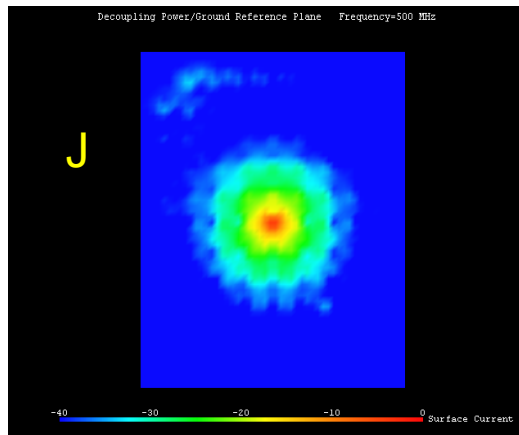


Fields and Currents

No Caps

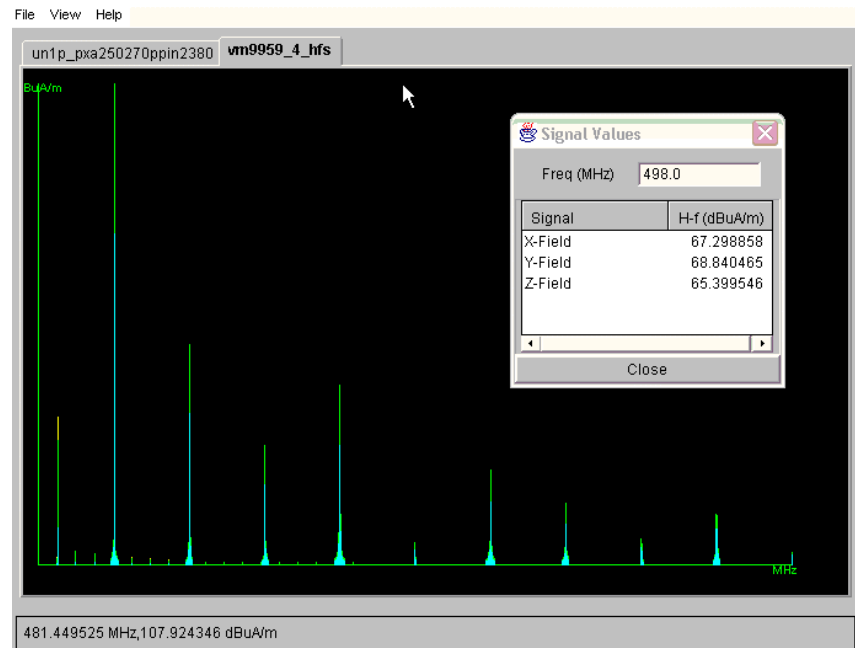


99 Caps



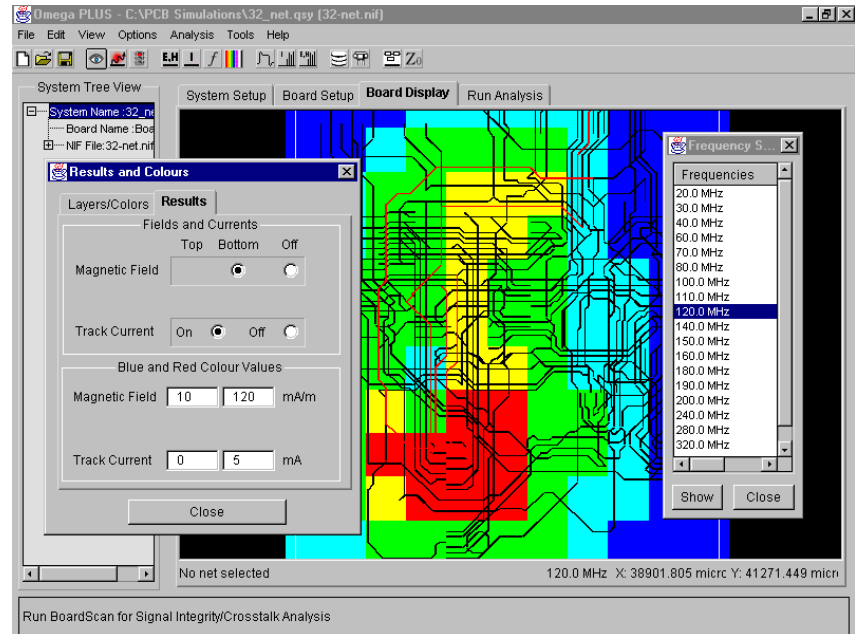
SI & EMI: Source Suppression

- Example of using a tool to simulate near fields a few mm above board
- Maximum magnetic field spectral values are plotted versus frequency
- We start by picking the “hottest” frequency



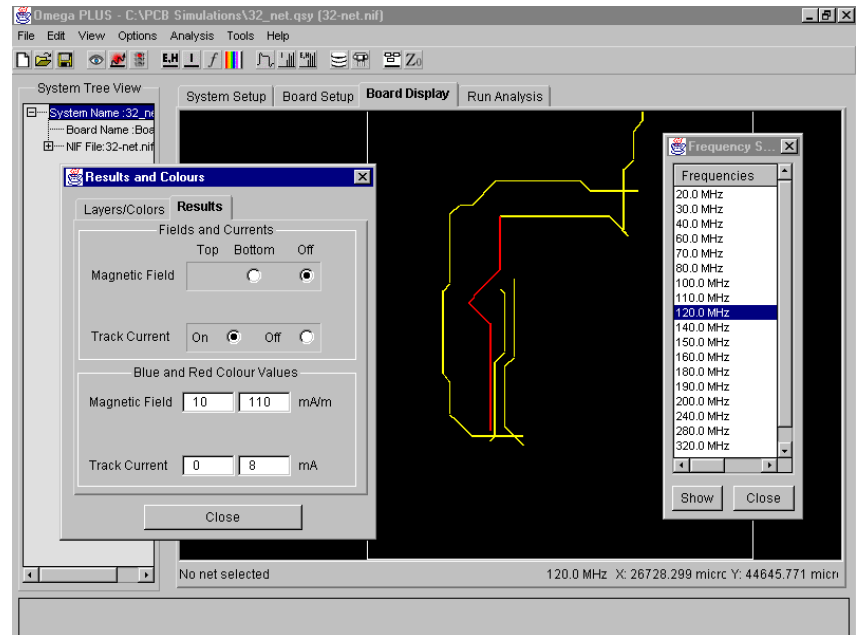
SI & EMI: Source Suppression (cont.)

- There are “hot” nets at 120 MHz
- Maximum magnetic field spectral values at the hot frequency are mapped and color coded



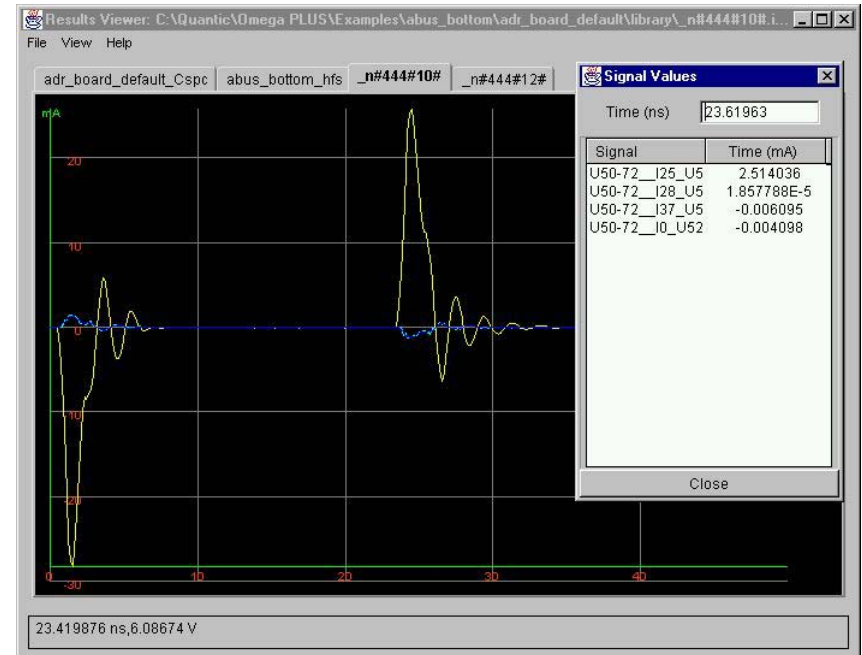
SI & EMI: Source Suppression (cont.)

- Next, the nets, and the particular portion of their etch, that are the principle cause of the emissions are identified



SI & EMI: Source Suppression (cont.)

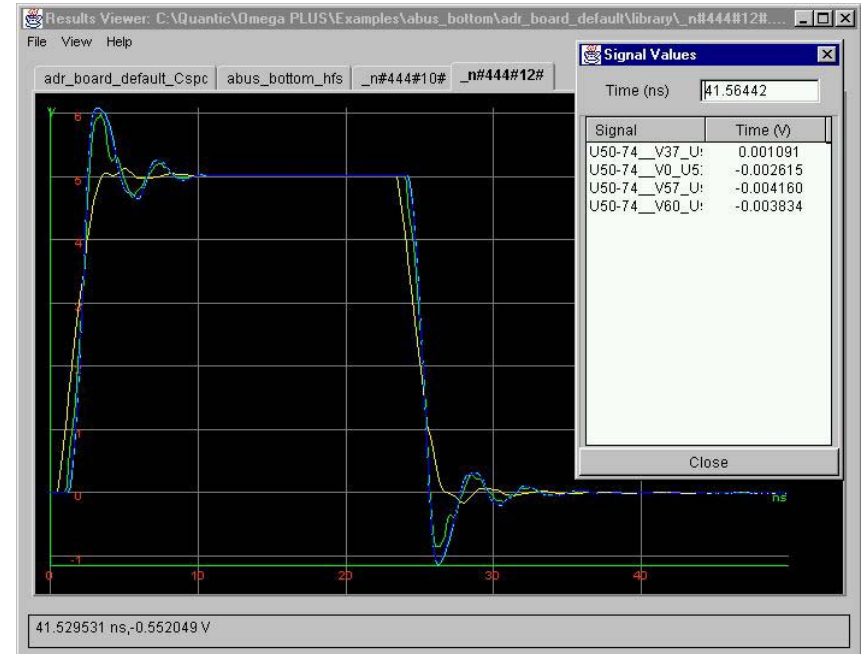
- Having isolated the nets, and the hot part of the etch, we look at their current waveforms



SI & EMI: Source Suppression (cont.)

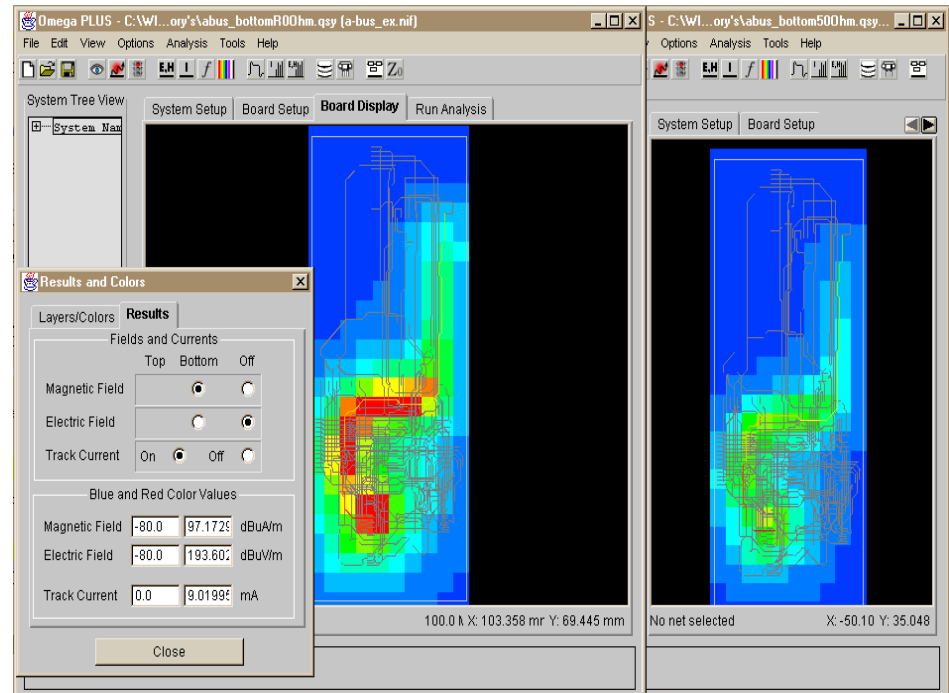
- The hot current is coming out of the driver, as it turns out.
- This is the corresponding voltage waveform
- Now, we begin to apply suppression techniques:

Are we dealing with driver edge rate, reflections, or what?
We want to apply the right cure.



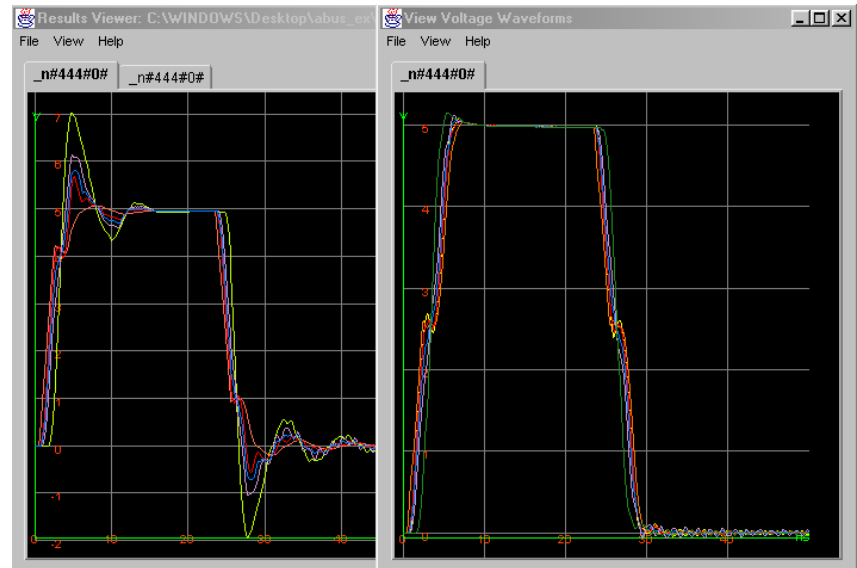
SI & EMI: Source Suppression (cont.)

- Here are some possible solutions:
 - termination
 - adjust driver edge rate
 - reroute net
 - adjust layer Zo
- This is an example of where emissions on this one net were reduced 5dB with a .05\$ resistor!

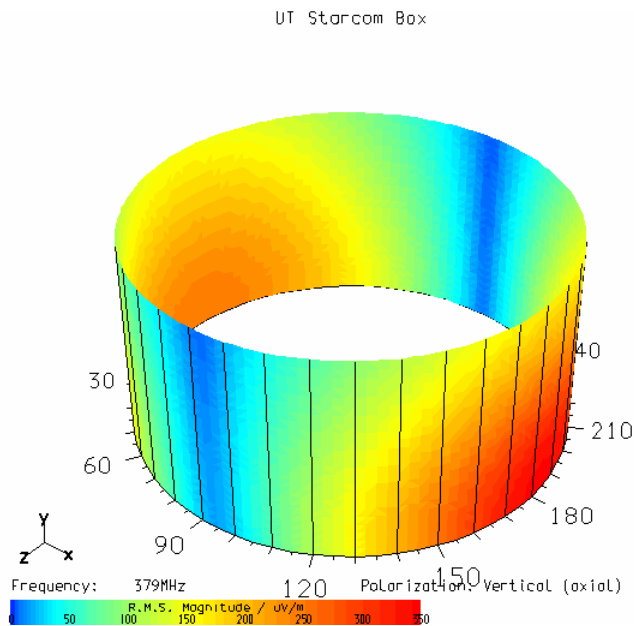


SI & EMI: Source Suppression (cont.)

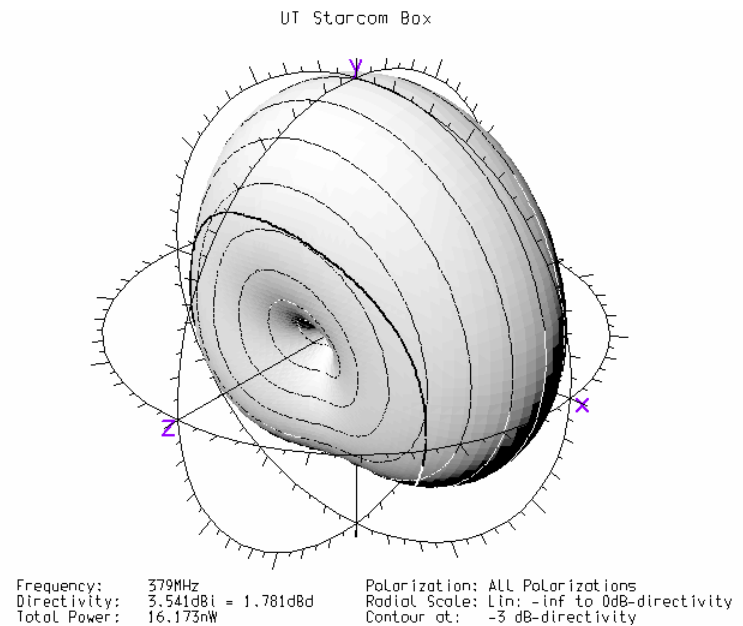
- Here is the before & after of adding a 50 Ω resistor.
Note:
 - ringing is really cleaned up - good for SI!
 - but, the rising/falling edge glitch is very bad news for SI!
 - We have an SI/EMI tradeoff to make!



Radiation at 379 MHz



3m cylinder scan



Far-Field radiation

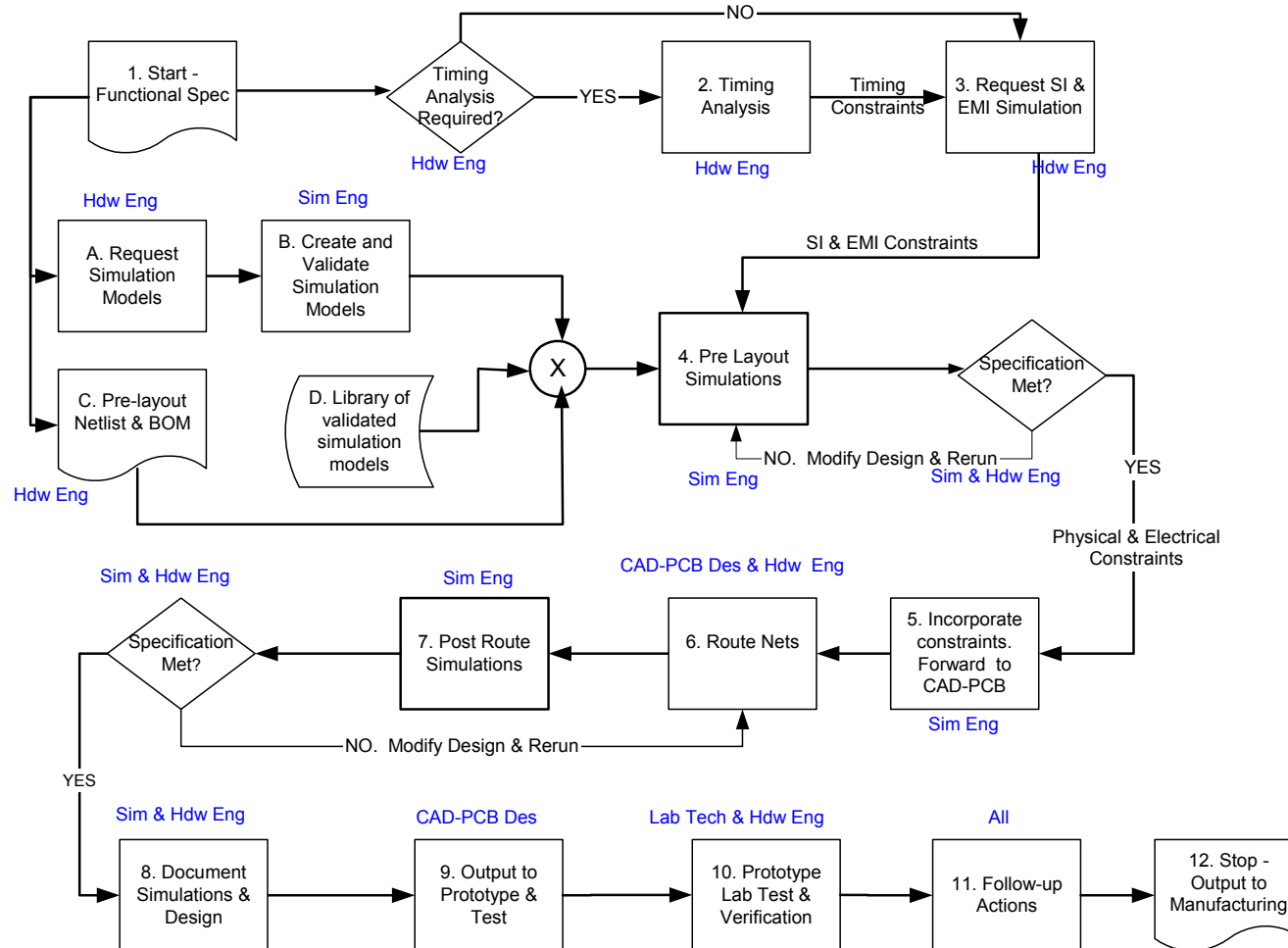
Past & Future Processes

Past	Future
Test & fix (Forget it)	Boards will be built correct by design
Debug board on bench	Debug model in computer
“What If” - Solder in resistors, etc.	“What If” - Sweep variables in computer
Current & Voltage Generators	E & H Generators
Generator internal impedance: R, C & L	Generator internal impedance: R, C & L and?
IC, Hybrid & MCM manufacturing, test & trim techniques: Ex.: Current mirrors, resistor laser trim, etc.	Apply these techniques to boards

Comparing SI and EMI

SI	EMI
Pre-layout Analysis: Schematic representation of transmission line models, etc.	Pre-layout Analysis: Schematic representation of model structures for certain defined cases
Output from Pre-layout: Topology - Template & Design Constraints	Output from Pre-layout: ? - Template & Design Constraints
Proprietary SPICE models → Behavioral IBIS (V-I, V-T, parasitics, etc.) models	Proprietary SPICE + pkg structure models → Behavioral ICEM 62014-3 (parasitics, Cd, CBT, M, IBM, etc.) models

Simulation Process Flow Chart



Summary

- A driver switches draws power from the power distribution system and puts a signal onto a net.
- Larger voltage and current fluctuations (with R, L, C, and G in components, boards and IC packages) result from:
 - faster switching and higher frequencies
 - higher currents to transfer the same charge in less time
- High speed effects:
 - transmission line reflections
 - losses, coupling between nets, and emissions
 - coupling to other PCBs, enclosures and beyond

Summary (cont.)

- Transient energy
 - reflects and re-reflects at discontinuities
 - couples as crosstalk to victim nets
 - appears in the power distribution system (power/ground bounce, conducted emissions)
 - coupling between printed wiring boards and into and through (emissions, EMI) enclosures

These unintended consequences cause noise on signals and can interfere with the proper operation of electronic equipment.

- The speed and power of the driver is the usual suspect
 - Driver modeling is critical to accurate simulation and design

Driver models are notoriously inaccurate!

“Simulation for the Suppression of PCB Emissions in Digital Telematics Devices” ITEM™ UPDATE 2002, p56

Scott Mee

Johnson Controls Inc.
Automotive Systems Group
EMC Product Compliance

Roy Leventhal

Leventhal Design &
Communications

Al Wexler, Mike Ventham

Quantic EMC Inc.

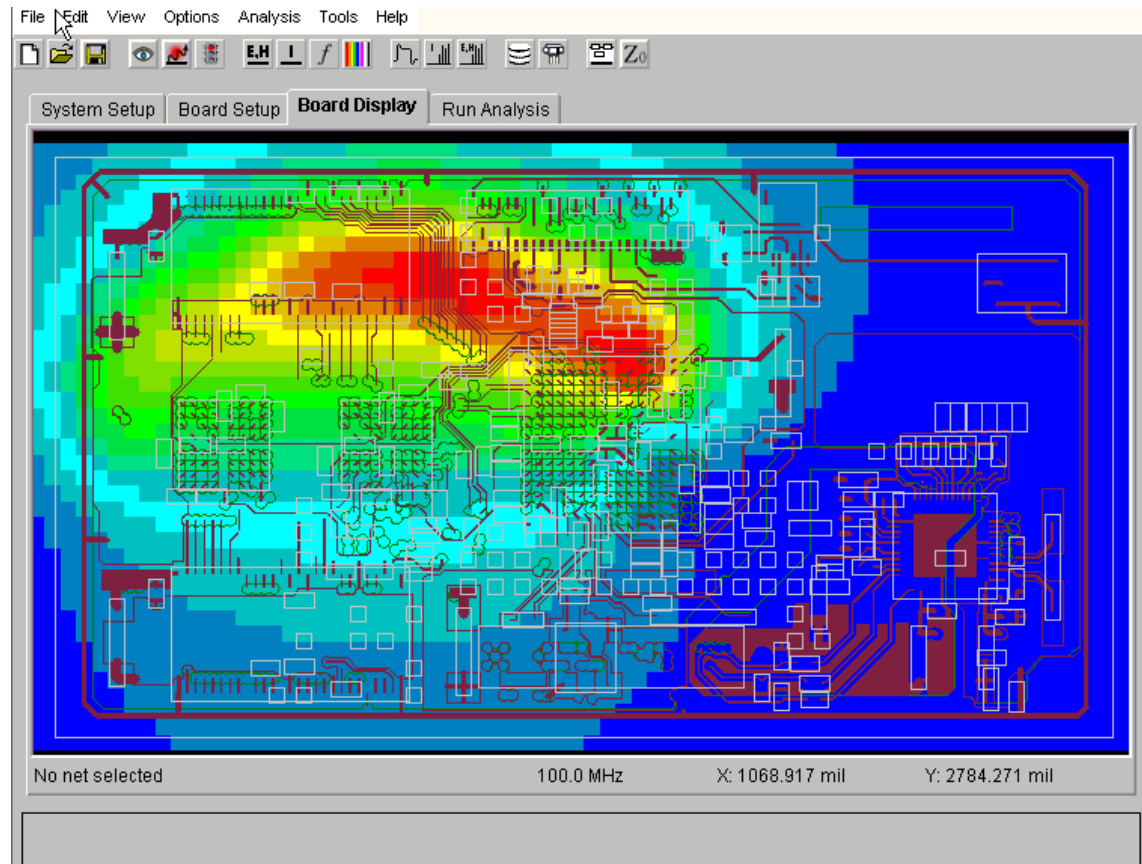
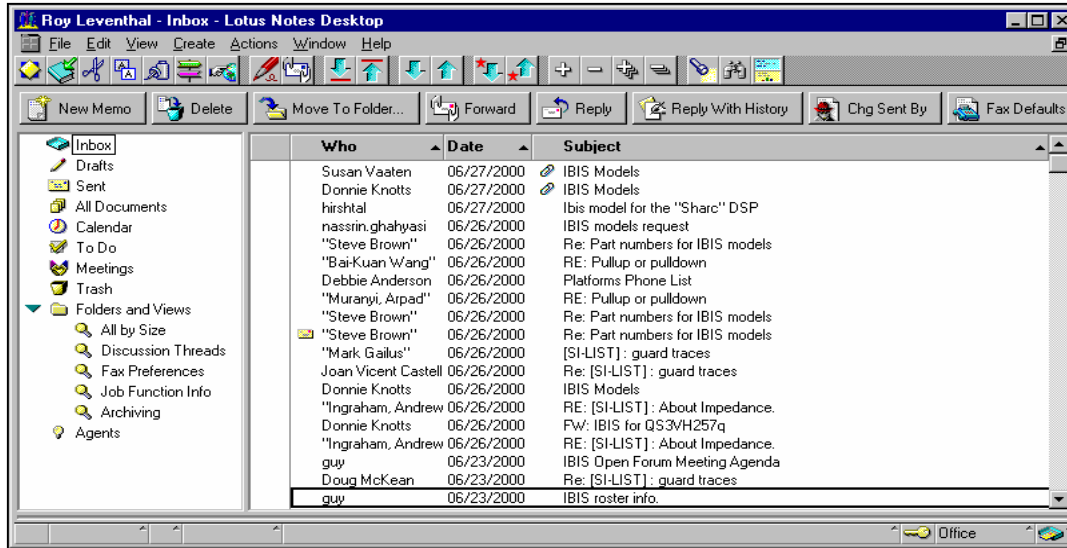


Image Courtesy of Johnson Controls Automotive, Inc. Used with permission

E-Mail Reflectors



A reflector is a moderated Email list server

To Post to	Send Email to
SI-List	si-list@freelists.org
IBIS	Ibis-users@eda.org

SI-List

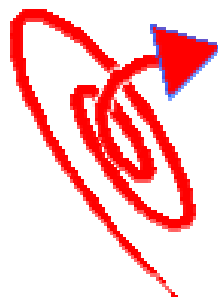
- Signal Integrity Mailing List:

This mailing list is for the discussion of signal integrity issues.

To subscribe to si-list, send an email message with your name and email address to:

- si-list-request@freelists.org
Put SUBSCRIBE in the SUBJECT

- List archives are viewable at:
<http://www.freelists.org/archives/si-list>
- Old list archives are viewable at: <http://www.qsl.net/wb6tpu>
- For gateway to archives & subscriber controls:
 - <http://www.freelists.org/webpage/si-list>



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